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12	PCH_MISC
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15	PCH_GND
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27	ISL95856 MOS_VCORE
28	ISL95856 MOS_VCCGT
29	VCCSA_VCCIO_VCCPLL
30	RT8120_DDR
31	RT8120_VPP
32	RT8120_PCH
33	DISCRETE POWER1
34	NCT3933
35	ATX_POWER , A_-PROCHOT

36	KB_MS_USB
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55	DP_IN SWITCH
56	HDMI_CONN
57	DP_OUT
58	M2M_32G
59	M2M_32G & STA4/5 SWITCH
60	M2P_32G
61	Realtek RTS5411 4port Hub-FRONT
62	N/A
63	EMI/ESD
64	NTC_MAP
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66	POWER零件使用表
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68	DUAL BIOS
69	U2_32G
70	N/A
71	EC ITE8792
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Gigabyte Technology

Title			Cover Sheet	
Size	Document Number		Rev	
Custom	GA-Z270X-GAMING 7		1.0	
Date:	Tuesday, November 22, 2016		Sheet	1 of 76

## Model Name: GA-Z270X-GAMING 7

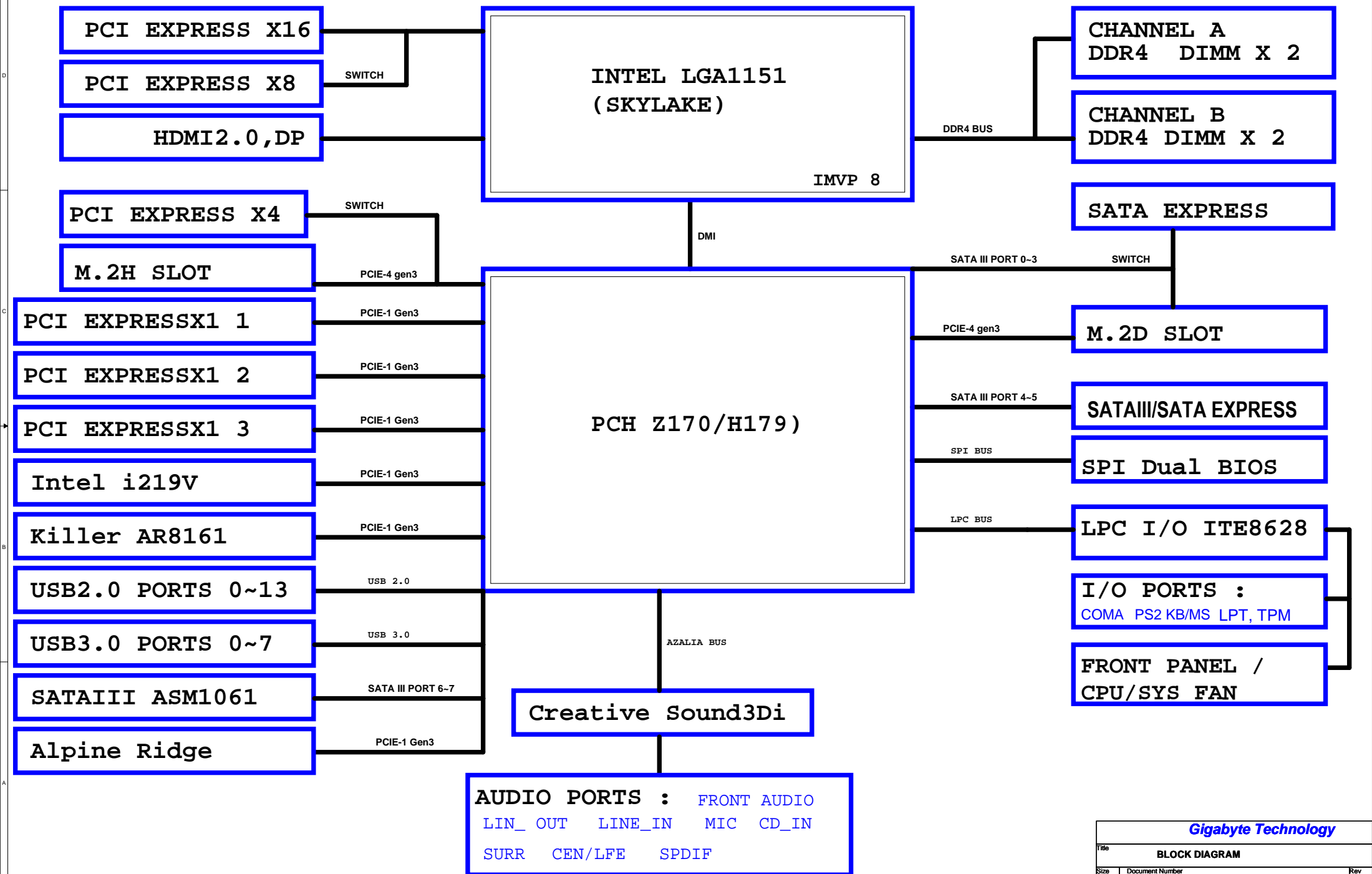
### Component value change history

Data	Change Item	Reason
2014/11/28 PCB:0.1	1. PCB first release	
	1. 高速訊號測試點移除	
	2. 0 OHM SHORT PAD	
	3. M_BIOS SOCKET移除	
	4. Remove JTAG	
0.2	1. 移除抗疏電阻替料 (重新轉NEW BOM for 抗疏電阻)	
	2. Update PCH_HS, MOS_HS, AUDIO_HS, REAR_HS	
	3. BTL1 UPDATE to "2.2uH/40A/CIN1310/FW/D"	
	4. 80P 螺柱改12KSF-F10303-11R	
	5. LED_C 料號:11NH2-000105-81R	
	6. CC12, CC13改10uF For LINE-IN Thd+N	
	7. NC2 27p --> 22p	
	8. ISL95856 load-line修改組值	
1.0A	1. 移除抗疏電阻替料 (重新轉NEW BOM for 抗疏電阻)	
	2. Update PCH_HS, MOS_HS, AUDIO_HS, REAR_HS	
	3. MCU_PH1不上或移除	
	4. SMD CHOKER改合金料號	
	5. 改ISL95866(包含R/C修改)	
	6. 背板PCB LED是否移除?	
	7. THU8上TPS65982 Rev.D (MOSFET要上件)	
	8. VCC1_0_PCH POWER SEQUENCY	
	9. Remove IO_LED CONTROL	
	10. M_BIOS SOCKET移除	
1.0B-0929	1. ECR31要上33/4/1	
	2. Modify VCC1_0_PCH POWER SEQUENCY	
1.0C	1. PCH 改量產料號:10HB1-03Z270-20R	
1.0D	1. Change MOSFET vendor Vishay --> ON	
	2. THESD3, THESD5, THESD7, THESD9, THESD4, THESD6, THESD8, THESD10 change to "10DET-510501-10R / NXP/PESD5V0H1BSF"	

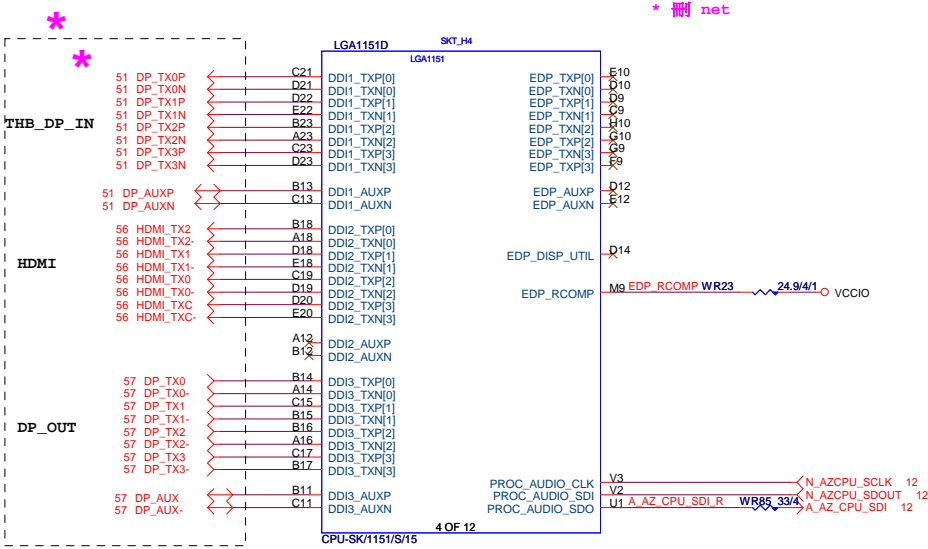
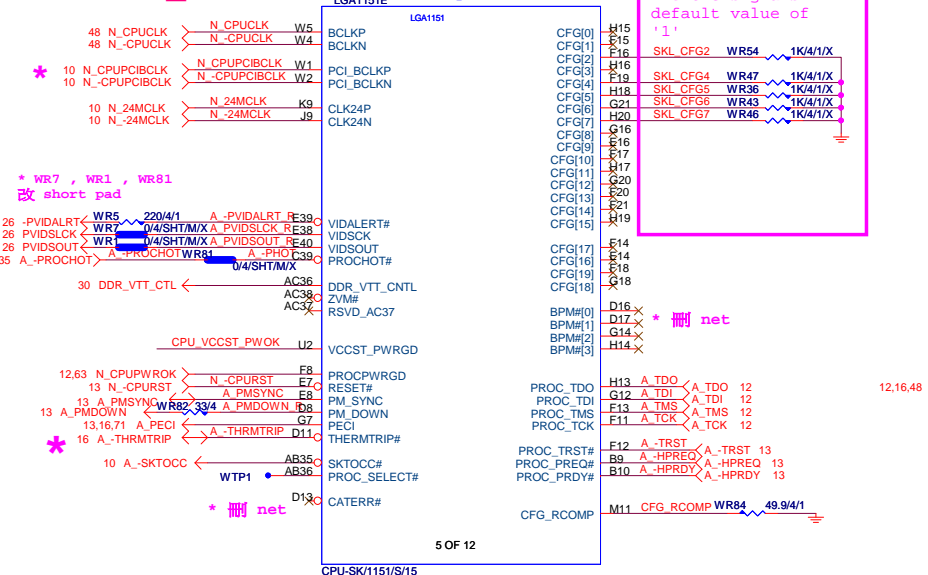
## Circuit or PCB layout change

DATE	Change Item	Reason
2014/11/28 PCB:0.1	1. PCB first release 2. 線路由GA-21704-SLI-01-1128B.DSN來修改	
2016/08/02 PCB:0.2	1. MCU_PH1 移除 2. Add logo "KILLER 2500" 3. BIOS_SW & SB 文字說明對調位置 4. Add NR85,NR86 for N_SUSCLK 5. SWFU3 SWAP pin 6. U2_32G pin.D6 connect "GND" 7. +12V切割線再往左移,增加+12V通道 8. DDR POWER INT1 remove DDR_VIN", "DDR_PHASE", "DDR_GND" 9. DDR POWER VCC 層 DDR_VIN", "DDR_PHASE", "DDR_GND"改空的 10. DAC_POWER CHOKE PHASE 改內層DUMMY (包含F_USB/R_USB) 11. 需要增加邊條測發光LEDx2pcs? (兩個定位孔請參考G1擺放) 12. DUAL BIOS模組線路修改 13. Debug LED位置請參考Note 14. BTBC16,18,19,20,THC146 改footprint "C0805" 15. 移除"PCB圖騰" 16. BSR21,BSR22對調 17. UPDATE LED CONTROL 18. DAR9 改走20mils , DAR39 從OUTPUT VCORE回來 , 19. A.R ADD N_GPP_H11 20. HUA17,29 SWAP , HAXT1,HAXT2 走等長 21. TTRT2移至DN_DQ2 22. 移除HDMI 2.0, DP-IN for Thunderbolt, PD 100W -> 27W 23. DD_DU1在POWER層包GND , DP_DC3的PH4_A VIA遠離DP訊號	
2016/08/04 PCB:0.3	1. MCU_PH1 移除 2. ADD LED MCUCD10-13 3. Update MCU LED control 4. 邊條LED是否有文字面擋住 5. UPDATE DUAL BIOS CONTROL (IO_GP84 --> B_SW) 6. PCB短路,MCU_LED和GND 7. 文字面修改:取消亮白和USB3.1_GEN2文字修改 8. REAR & AUDIO 裝甲UPDATE footprint 9. THFB1 footprint update "FB0402-RH" 10. Update REAR_HS , AUDIO_HS footprint 11. Add VPP_25V ECR161 , MABC8 change "R0402-2" 12. Remove LED_PCH 13. Add "THB3" logo 14. ECO pin "N_GPP_C8 --> N_GPP_B20" , PUMP2 "N_GPP_B20--> N_GPP_B11" 15. 0 OHM change to short pad 16. Remove NR86 , TPM pin20 change to N.C.	
2016/09/14 PCB:1.0	1. 0 ohm short pad (R0402/R0603/排阻) 2. WR59,WR60,WR61 改"R0402-2" 3. PUMP1 --> SYS_FAN5_PUMP , PUMP2 --> SYS_FAN6_PUMP 4. PCB圖騰增加斜紋灰色 5. OC/ECO/PW_SW文字面擺設修改 (變小) 6. EC_TEMP2/CLR_CMOS文字面修改, 7. LED_C pin1說明 8. AMP +12V / -12V disable save mode 9. LED Beat ADD "N_GPP_D10" , Remove PCIE SLOT CONTROL	
2016/ PCB:1.01	1. RST_SW & CMOS_SW 文字位置調整 2. ITE8792 GP73 add "N_-RSMRST" 3. Add VIN CAP DCCL,DCC2,DCC3,DCC51,DCC52,DCC53,DCC54,DCC55 4. DDR 的T型訊號請由4mils改成4.5mils 線?	

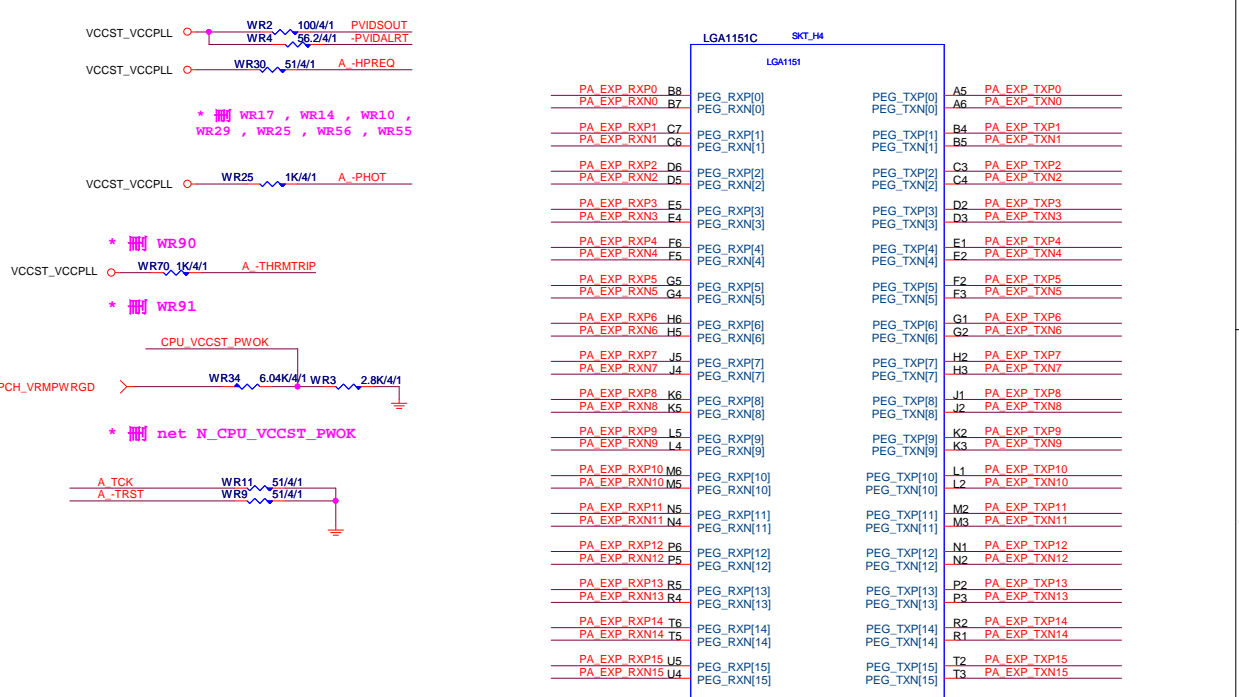
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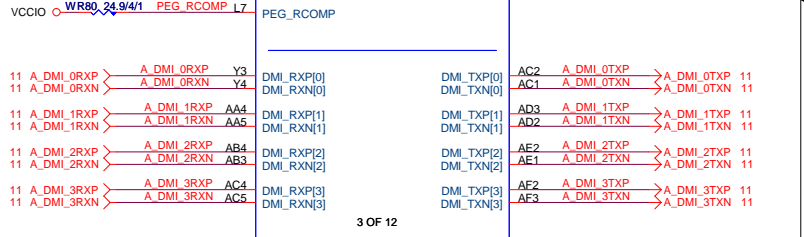
## From SKL\_0.2B



```
G-15u : (CPU-SK/1151/S/15)
10SC1-F01151-11R / 10SC1-F01151-12R
G-FL : (CPU-SK/1151/S/GF)
10SC1-F01151-21R / 10SC1-F01151-22R
```



Bifurcation Config.	Signals Lanes		
	CFG[6]	CFG[5]	CFG[2]
1x16	1	1	1
1x16 Reversed	1	1	0
2x8	1	0	1
2x8 Reversed	1	0	0
1x8+2x4	0	0	1
1x8+2x4 Reversed	0	0	0



PA_EXP_TXP[0..15]	>>	PA_EXP_TXP[0..15]	19,21
PA_EXP_TXN[0..15]	>>	PA_EXP_TXN[0..15]	19,21
PA_EXP_RXP[0..15]	>>	PA_EXP_RXP[0..15]	19,21
PA_EXP_RXN[0..15]	>>	PA_EXP_RXN[0..15]	19,21

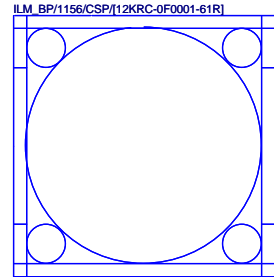
W=12 mil out of CPU  
S=15 mil out of CPU

\* 改DDR4 net

LGA1151A			SKT_H4		
LGA1151			LGA1151		
MDA0 AE38	DDR0_DQ[0]	DDR0_CK[0]	AW18 M_DCLKA0	→	M_DCLKA0 8
MDA1 AE37	DDR0_DQ[1]	DDR0_CK[1]	AW18 M_DCLKA0	→	M_DCLKA0 8
MDA2 AG38	DDR0_DQ[2]	DDR0_CK[2]	AW17 M_DCLKA1	→	M_DCLKA1 8
MDA3 AG37	DDR0_DQ[3]	DDR0_CK[3]	AW17 M_DCLKA1	→	M_DCLKA1 8
MDA4 AE39	DDR0_DQ[4]	DDR0_CK[4]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA5 AE39	DDR0_DQ[5]	DDR0_CK[5]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA6 AE39	DDR0_DQ[6]	DDR0_CK[6]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA7 AG40	DDR0_DQ[7]	DDR0_CK[7]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA8 AJ38	DDR0_DQ[8]	DDR0_CK[8]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA9 AJ37	DDR0_DQ[9]	DDR0_CK[9]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA10 AL38	DDR0_DQ[10]	DDR0_CK[10]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA11 AL37	DDR0_DQ[11]	DDR0_CK[11]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA12 AJ40	DDR0_DQ[12]	DDR0_CK[12]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA13 AJ39	DDR0_DQ[13]	DDR0_CK[13]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA14 AL39	DDR0_DQ[14]	DDR0_CK[14]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA15 AL40	DDR0_DQ[15]	DDR0_CK[15]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA16 AN38	DDR0_DQ[16]	DDR0_CK[16]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA17 AN38	DDR0_DQ[17]	DDR0_CK[17]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA18 AR38	DDR0_DQ[18]	DDR0_CK[18]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA19 AR37	DDR0_DQ[19]	DDR0_CK[19]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA20 AN39	DDR0_DQ[20]	DDR0_CK[20]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA21 AN37	DDR0_DQ[21]	DDR0_CK[21]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA22 AR39	DDR0_DQ[22]	DDR0_CK[22]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA23 AR40	DDR0_DQ[23]	DDR0_CK[23]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA24 AW37	DDR0_DQ[24]	DDR0_CK[24]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA25 AU38	DDR0_DQ[25]	DDR0_CK[25]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA26 AV35	DDR0_DQ[26]	DDR0_CK[26]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA27 AW35	DDR0_DQ[27]	DDR0_CK[27]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA28 AW37	DDR0_DQ[28]	DDR0_CK[28]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA29 AV37	DDR0_DQ[29]	DDR0_CK[29]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA30 AT35	DDR0_DQ[30]	DDR0_CK[30]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA31 AU35	DDR0_DQ[31]	DDR0_CK[31]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA32 AY8	DDR0_DQ[32]	DDR0_CK[32]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA33 AW8	DDR0_DQ[33]	DDR0_CK[33]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA34 AV6	DDR0_DQ[34]	DDR0_CK[34]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA35 AU6	DDR0_DQ[35]	DDR0_CK[35]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA36 AU8	DDR0_DQ[36]	DDR0_CK[36]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA37 AV8	DDR0_DQ[37]	DDR0_CK[37]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA38 AV6	DDR0_DQ[38]	DDR0_CK[38]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA39 AV4	DDR0_DQ[39]	DDR0_CK[39]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA40 AV4	DDR0_DQ[40]	DDR0_CK[40]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA41 AV4	DDR0_DQ[41]	DDR0_CK[41]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA42 AT1	DDR0_DQ[42]	DDR0_CK[42]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA43 AT2	DDR0_DQ[43]	DDR0_CK[43]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA44 AV3	DDR0_DQ[44]	DDR0_CK[44]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA45 AW4	DDR0_DQ[45]	DDR0_CK[45]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA46 AT4	DDR0_DQ[46]	DDR0_CK[46]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA47 AT3	DDR0_DQ[47]	DDR0_CK[47]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA48 AP2	DDR0_DQ[48]	DDR0_CK[48]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA49 AP3	DDR0_DQ[49]	DDR0_CK[49]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA50 AM4	DDR0_DQ[50]	DDR0_CK[50]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA51 AM3	DDR0_DQ[51]	DDR0_CK[51]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA52 AP4	DDR0_DQ[52]	DDR0_CK[52]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA53 AM2	DDR0_DQ[53]	DDR0_CK[53]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA54 AP1	DDR0_DQ[54]	DDR0_CK[54]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA55 AM1	DDR0_DQ[55]	DDR0_CK[55]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA56 AK3	DDR0_DQ[56]	DDR0_CK[56]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA57 AH1	DDR0_DQ[57]	DDR0_CK[57]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA58 AK4	DDR0_DQ[58]	DDR0_CK[58]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA59 AH2	DDR0_DQ[59]	DDR0_CK[59]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA60 AH4	DDR0_DQ[60]	DDR0_CK[60]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA61 AK2	DDR0_DQ[61]	DDR0_CK[61]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA62 AH3	DDR0_DQ[62]	DDR0_CK[62]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA63 AK1	DDR0_DQ[63]	DDR0_CK[63]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA ECC0 AU33	DDR0_ECC[0]	DDR0_ECC[0]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA ECC1 AT33	DDR0_ECC[1]	DDR0_ECC[1]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA ECC2 AW33	DDR0_ECC[2]	DDR0_ECC[2]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA ECC3 AV31	DDR0_ECC[3]	DDR0_ECC[3]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA ECC4 AU31	DDR0_ECC[4]	DDR0_ECC[4]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA ECC5 AV33	DDR0_ECC[5]	DDR0_ECC[5]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA ECC6 AW31	DDR0_ECC[6]	DDR0_ECC[6]	AW16 M_DCLKA2	→	M_DCLKA2 8
MDA ECC7 AY31	DDR0_ECC[7]	DDR0_ECC[7]	AW16 M_DCLKA2	→	M_DCLKA2 8

8 MDA\_ECC[0..7] ↔ MDA ECC[0..7]

LGA1151



Need check the new CPU ME

CPU-SK/1151/S/15

1 OF 12

LGA1151B			SKT_H4		
LGA1151			LGA1151		
MDB0 AD34	DDR1_DQ[0]	DDR1_CK[0]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB1 AD35	DDR1_DQ[1]	DDR1_CK[1]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB2 AG35	DDR1_DQ[2]	DDR1_CK[2]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB3 AH35	DDR1_DQ[3]	DDR1_CK[3]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB4 AE35	DDR1_DQ[4]	DDR1_CK[4]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB5 AE34	DDR1_DQ[5]	DDR1_CK[5]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB6 AE34	DDR1_DQ[6]	DDR1_CK[6]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB7 AH34	DDR1_DQ[7]	DDR1_CK[7]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB8 AK35	DDR1_DQ[8]	DDR1_CK[8]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB9 AL35	DDR1_DQ[9]	DDR1_CK[9]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB10 AL32	DDR1_DQ[10]	DDR1_CK[10]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB11 AL32	DDR1_DQ[11]	DDR1_CK[11]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB12 AK34	DDR1_DQ[12]	DDR1_CK[12]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB13 AL34	DDR1_DQ[13]	DDR1_CK[13]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB14 AK31	DDR1_DQ[14]	DDR1_CK[14]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB15 AL31	DDR1_DQ[15]	DDR1_CK[15]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB16 AE35	DDR1_DQ[16]	DDR1_CK[16]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB17 AN35	DDR1_DQ[17]	DDR1_CK[17]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB18 AN32	DDR1_DQ[18]	DDR1_CK[18]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB19 AP32	DDR1_DQ[19]	DDR1_CK[19]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB20 AN34	DDR1_DQ[20]	DDR1_CK[20]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB21 AE34	DDR1_DQ[21]	DDR1_CK[21]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB22 AE34	DDR1_DQ[22]	DDR1_CK[22]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB23 AP31	DDR1_DQ[23]	DDR1_CK[23]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB24 AL29	DDR1_DQ[24]	DDR1_CK[24]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB25 AM29	DDR1_DQ[25]	DDR1_CK[25]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB26 AE29	DDR1_DQ[26]	DDR1_CK[26]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB27 AE29	DDR1_DQ[27]	DDR1_CK[27]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB28 AE28	DDR1_DQ[28]	DDR1_CK[28]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB29 AL28	DDR1_DQ[29]	DDR1_CK[29]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB30 AR28	DDR1_DQ[30]	DDR1_CK[30]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB31 AP28	DDR1_DQ[31]	DDR1_CK[31]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB32 AB12	DDR1_DQ[32]	DDR1_CK[32]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB33 AP12	DDR1_DQ[33]	DDR1_CK[33]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB34 AM13	DDR1_DQ[34]	DDR1_CK[34]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB35 AL13	DDR1_DQ[35]	DDR1_CK[35]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB36 AR13	DDR1_DQ[36]	DDR1_CK[36]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB37 AP13	DDR1_DQ[37]	DDR1_CK[37]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB38 AM12	DDR1_DQ[38]	DDR1_CK[38]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB39 AP10	DDR1_DQ[39]	DDR1_CK[39]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB40 AR10	DDR1_DQ[40]	DDR1_CK[40]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB41 AR10	DDR1_DQ[41]	DDR1_CK[41]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB42 AR7	DDR1_DQ[42]	DDR1_CK[42]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB43 AP7	DDR1_DQ[43]	DDR1_CK[43]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB44 AP9	DDR1_DQ[44]	DDR1_CK[44]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB45 AP9	DDR1_DQ[45]	DDR1_CK[45]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB46 AR6	DDR1_DQ[46]	DDR1_CK[46]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB47 AP6	DDR1_DQ[47]	DDR1_CK[47]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB48 AM10	DDR1_DQ[48]	DDR1_CK[48]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB49 AL10	DDR1_DQ[49]	DDR1_CK[49]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB50 AM7	DDR1_DQ[50]	DDR1_CK[50]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB51 AL7	DDR1_DQ[51]	DDR1_CK[51]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB52 AM9	DDR1_DQ[52]	DDR1_CK[52]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB53 AL9	DDR1_DQ[53]	DDR1_CK[53]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB54 AM6	DDR1_DQ[54]	DDR1_CK[54]	AW20 M_DCLKB0	→	M_DCLKB0 9
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MDB57 AJ7	DDR1_DQ[57]	DDR1_CK[57]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB58 AE6	DDR1_DQ[58]	DDR1_CK[58]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB59 AE7	DDR1_DQ[59]	DDR1_CK[59]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB60 AH7	DDR1_DQ[60]	DDR1_CK[60]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB61 AH6	DDR1_DQ[61]	DDR1_CK[61]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB62 AE7	DDR1_DQ[62]	DDR1_CK[62]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB63 AE6	DDR1_DQ[63]	DDR1_CK[63]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB ECC0 AR25	DDR1_ECC[0]	DDR1_ECC[0]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB ECC1 AR28	DDR1_ECC[1]	DDR1_ECC[1]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB ECC2 AM26	DDR1_ECC[2]	DDR1_ECC[2]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB ECC3 AM25	DDR1_ECC[3]	DDR1_ECC[3]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB ECC4 AP26	DDR1_ECC[4]	DDR1_ECC[4]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB ECC5 AP25	DDR1_ECC[5]	DDR1_ECC[5]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB ECC6 AL25	DDR1_ECC[6]	DDR1_ECC[6]	AW20 M_DCLKB0	→	M_DCLKB0 9
MDB ECC7 AL26	DDR1_ECC[7]	DDR1_ECC[7]	AW20 M_DCLKB0	→	M_DCLKB0 9

9 MDB\_ECC[0..7] ↔ MDB ECC[0..7]

DDR CHANNEL B

CPU-SK/1151/S/15

8 MODT\_A[0..3] ↔ MODT A[0..3]  
9 MODT\_B[0..3] ↔ MODT B[0..3]  
8 MDA[0..63] ↔ MDA[0..63]  
9 MDB[0..63] ↔ MDB[0..63]  
8 M\_DQSA[0..7] ↔ M\_DQSA[0..7]  
8 M\_-DQSA[0..7] ↔ M\_-DQSA[0..7]  
8 MAAA[0..16] ↔ MAAA[0..16]  
9 MAAB[0..16] ↔ MAAB[0..16]  
9 M\_DQSB[0..7] ↔ M\_DQSB[0..7]  
9 M\_-DQSB[0..7] ↔ M\_-DQSB[0..7]

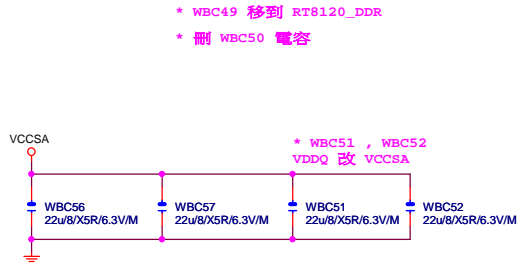
Gigabyte Technology

CPU LGA1151-B

GA-Z270X-GAMING 7

Rev 1.0

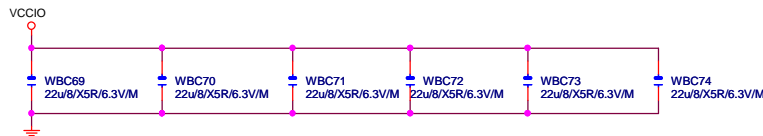
Date: Tuesday, November 22, 2016 Sheet 5 of 76



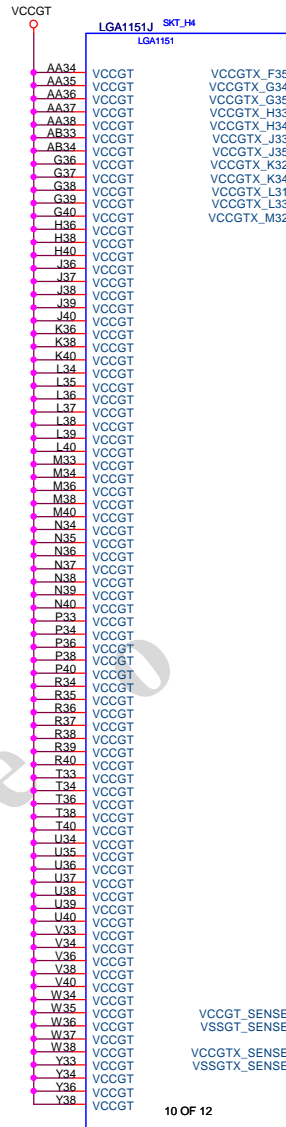
\* 刪 WBC124 , WBC125 , WBC126 , WBC127 電容

CPU POWER

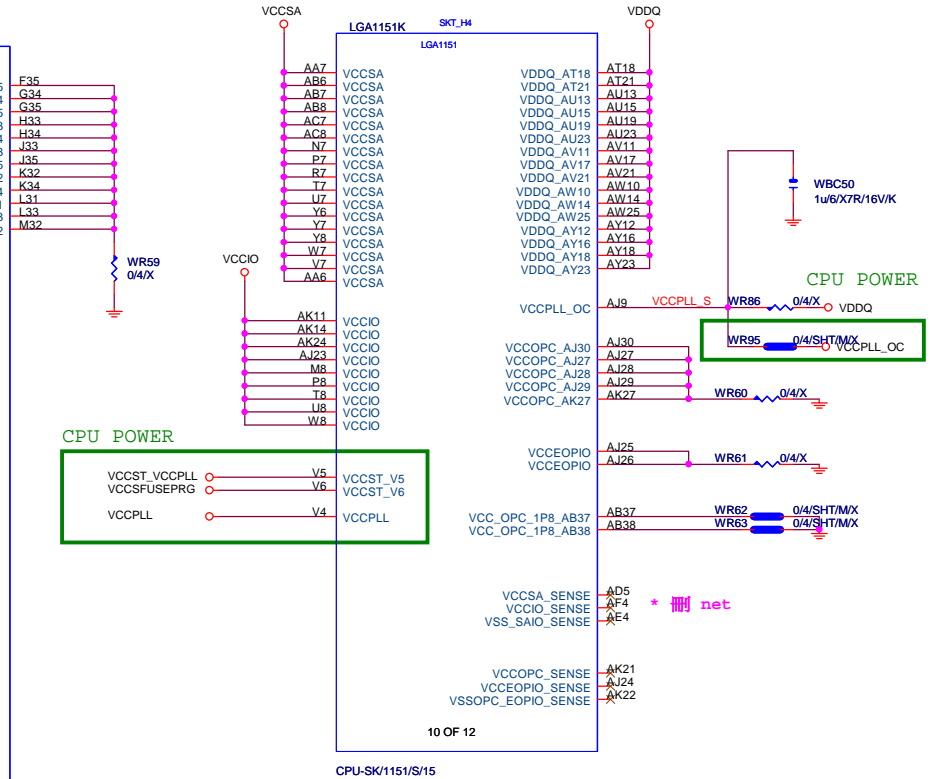
\* WR94 , WR59 , WR86 , WR60 ,  
WR61 , WR62 , WR63 改 short  
pad



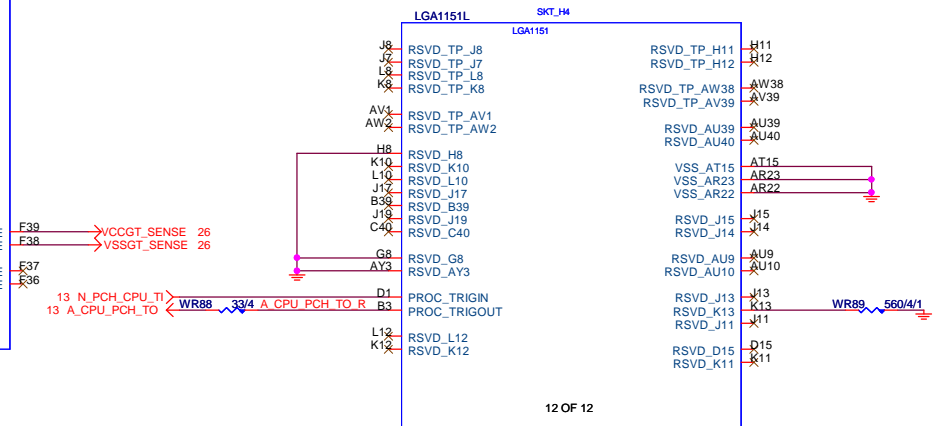
\* 刪 VCCGT 電容



CPU-SK/1151/S/15



CPU-SK/1151/S/15



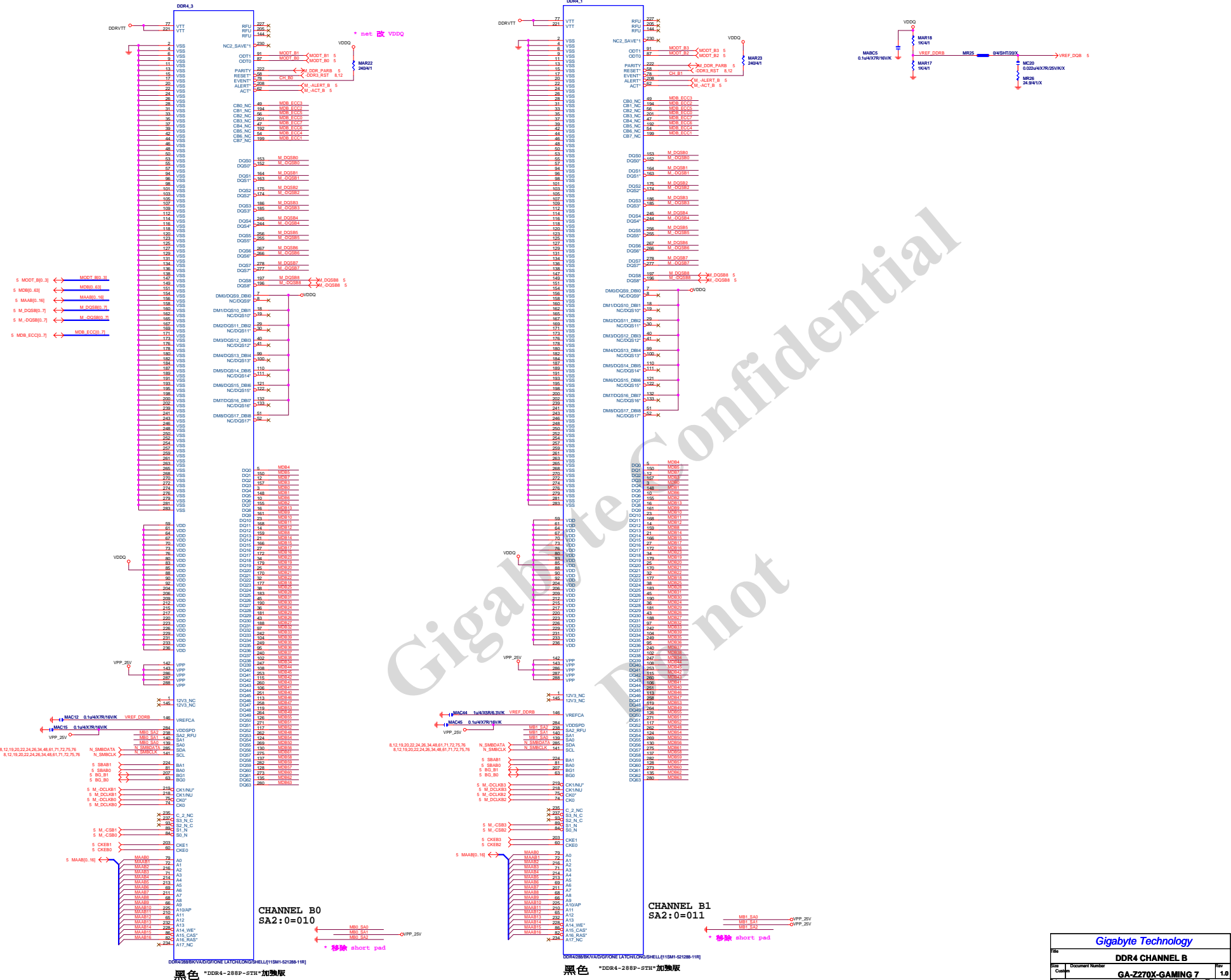
CPU-SK/1151/S/15











DOR4.3

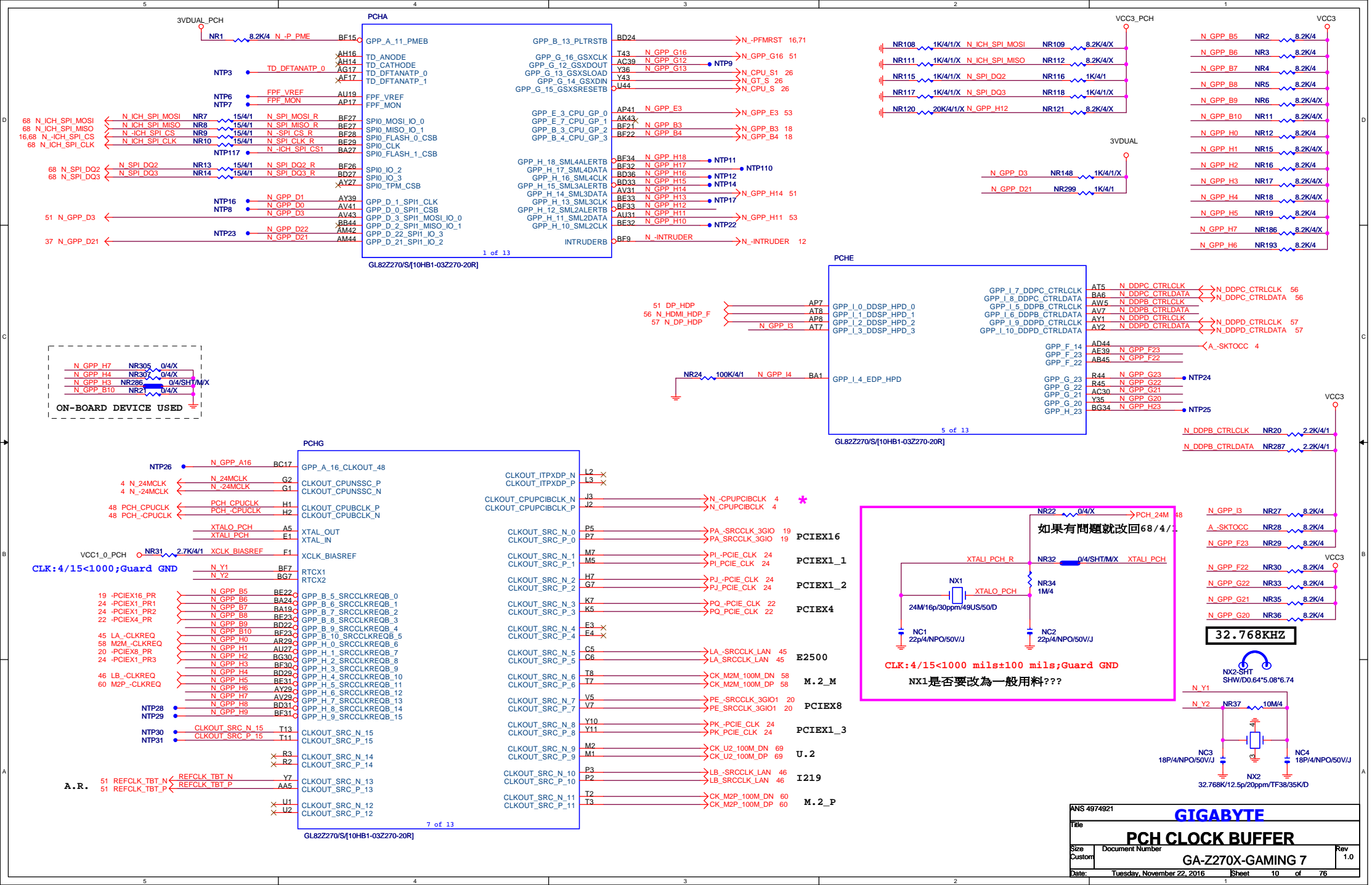
DOR4.1

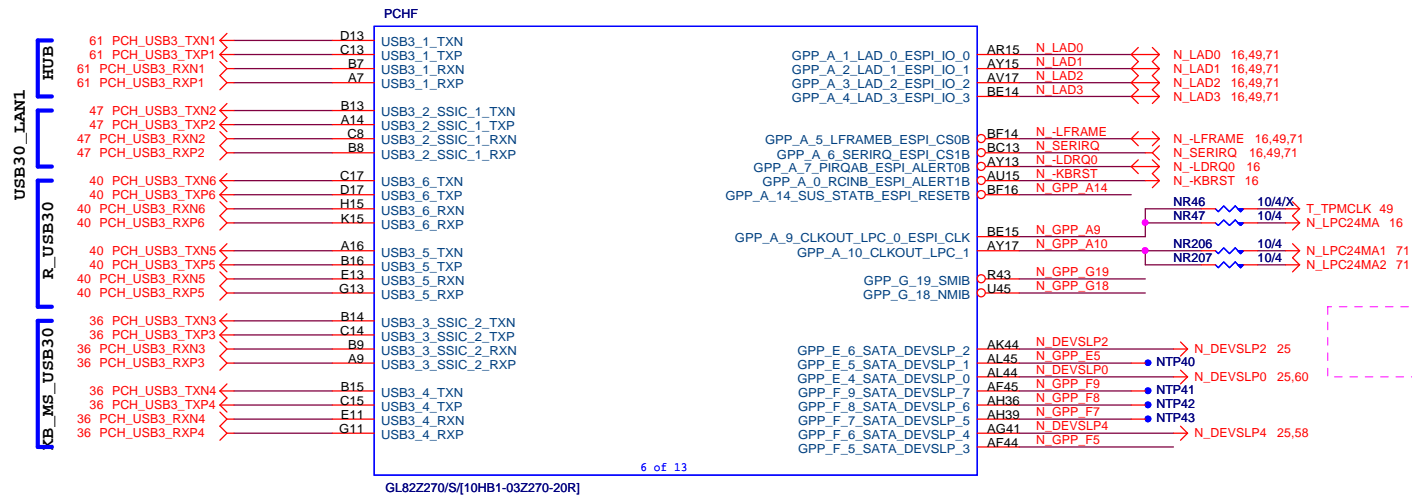
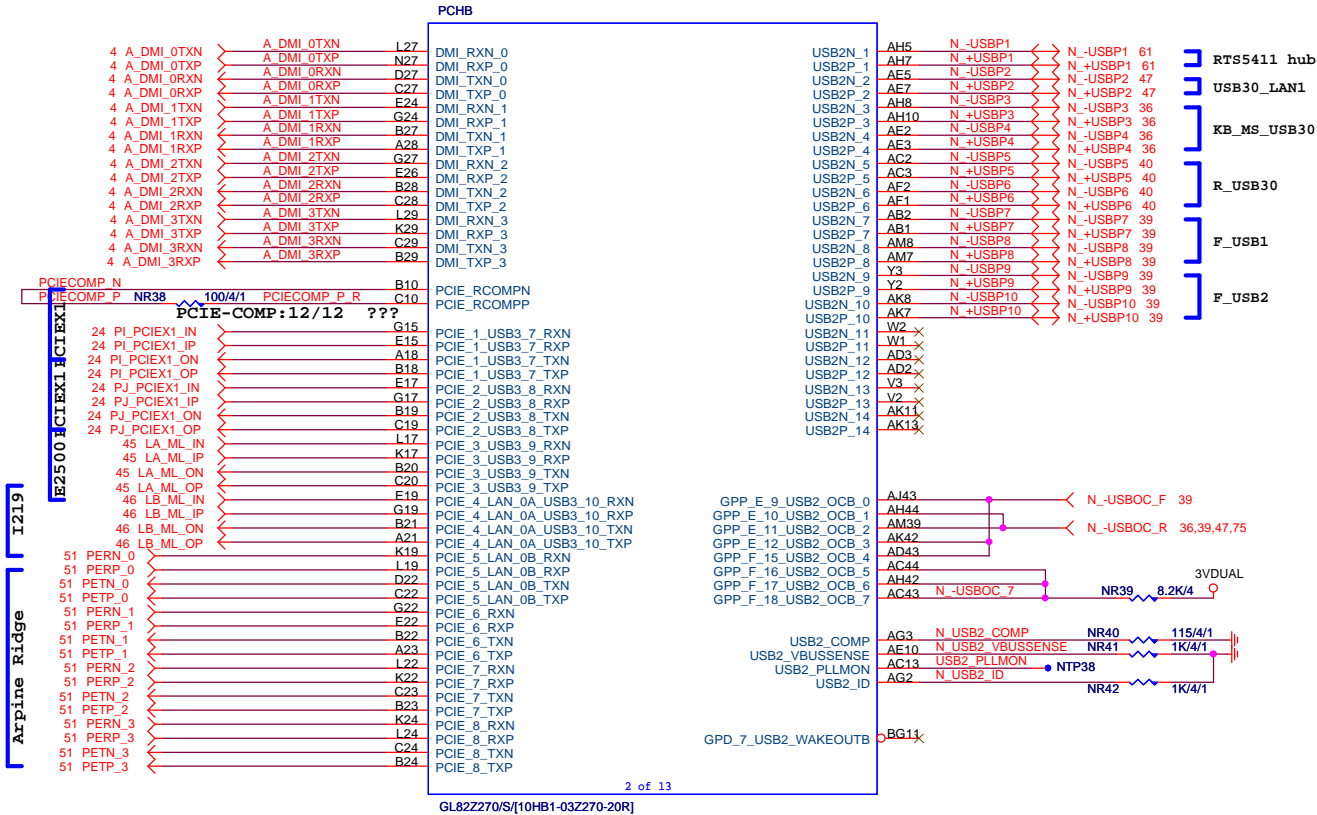
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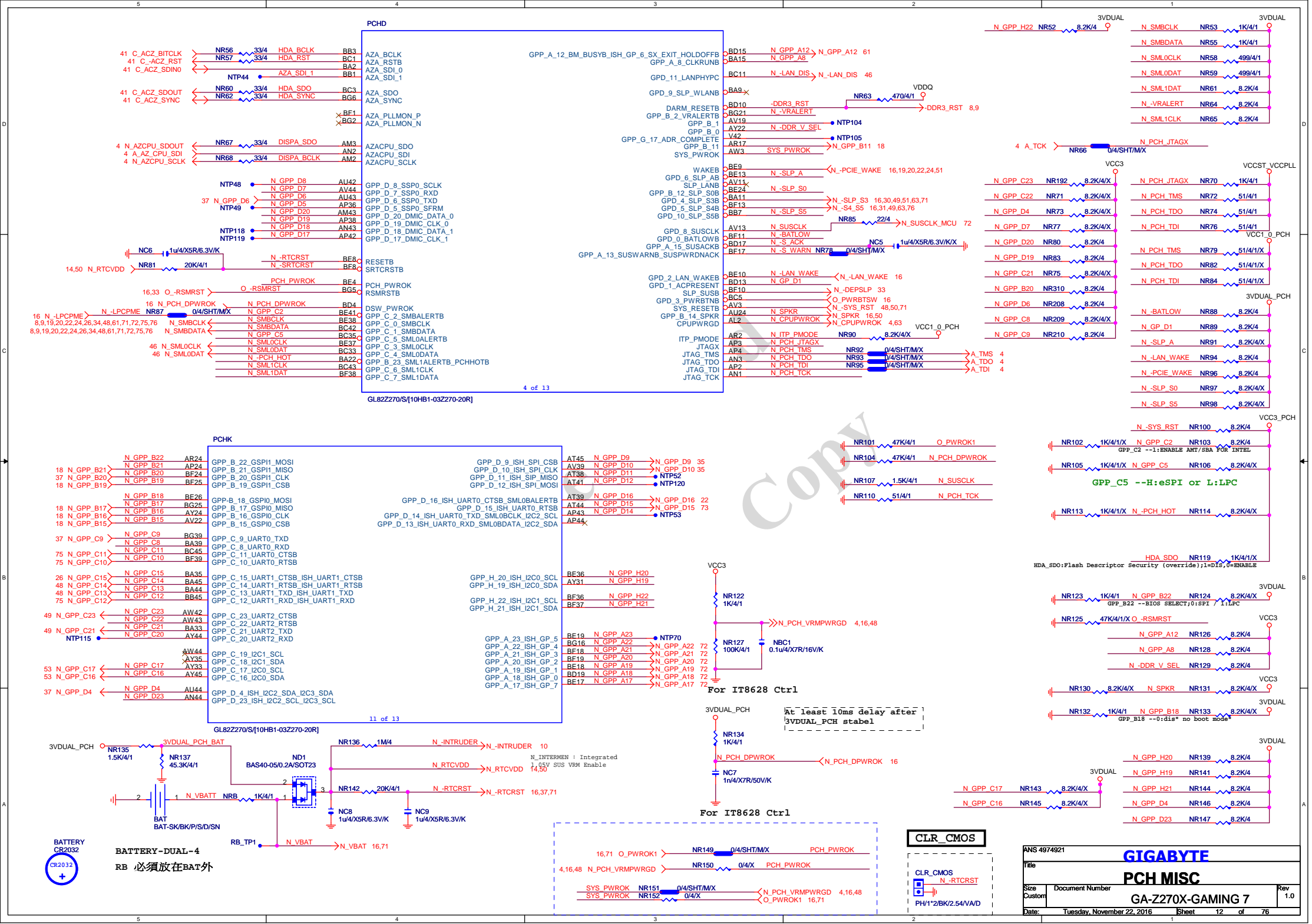
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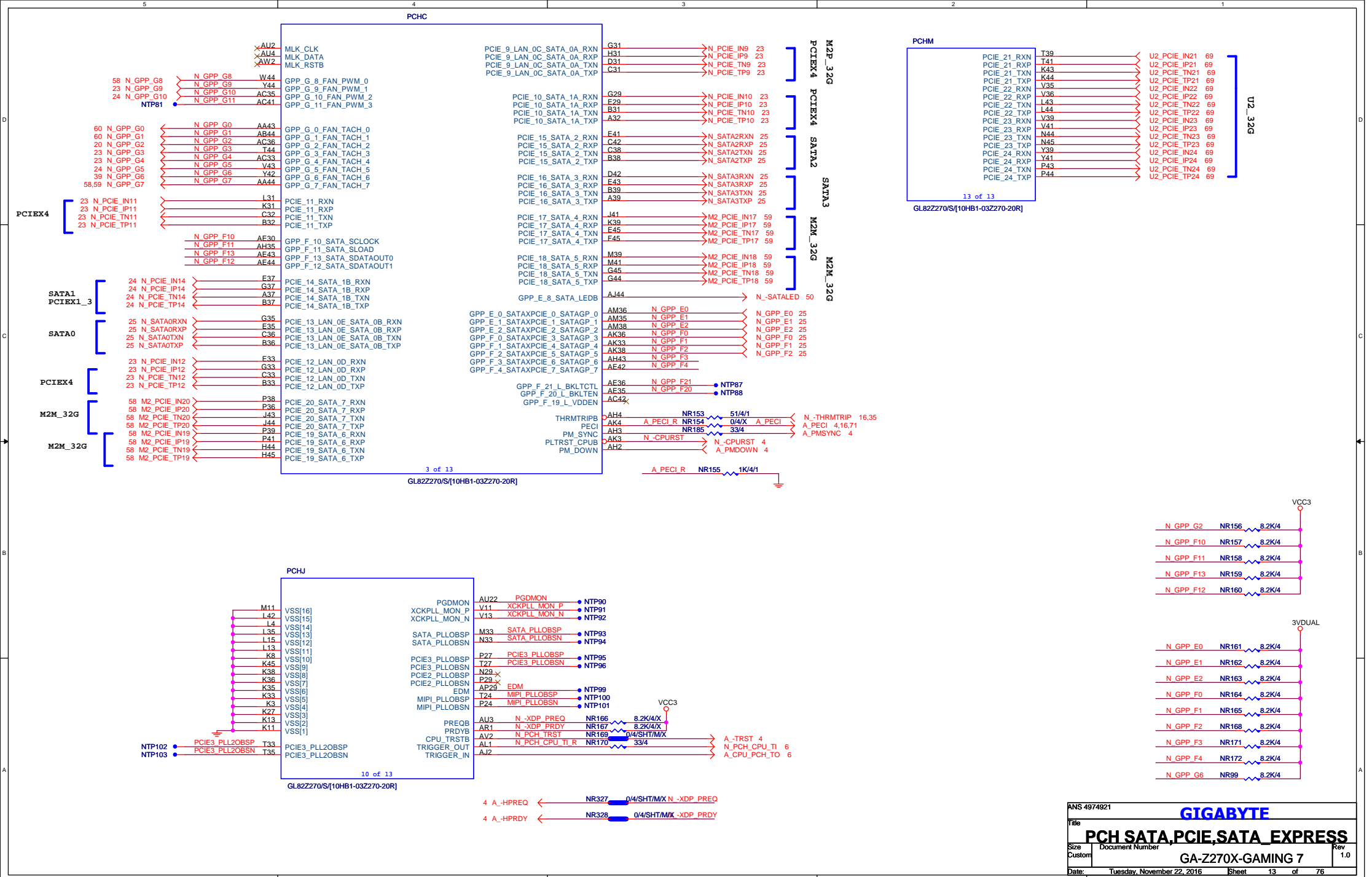
黑色

黑色

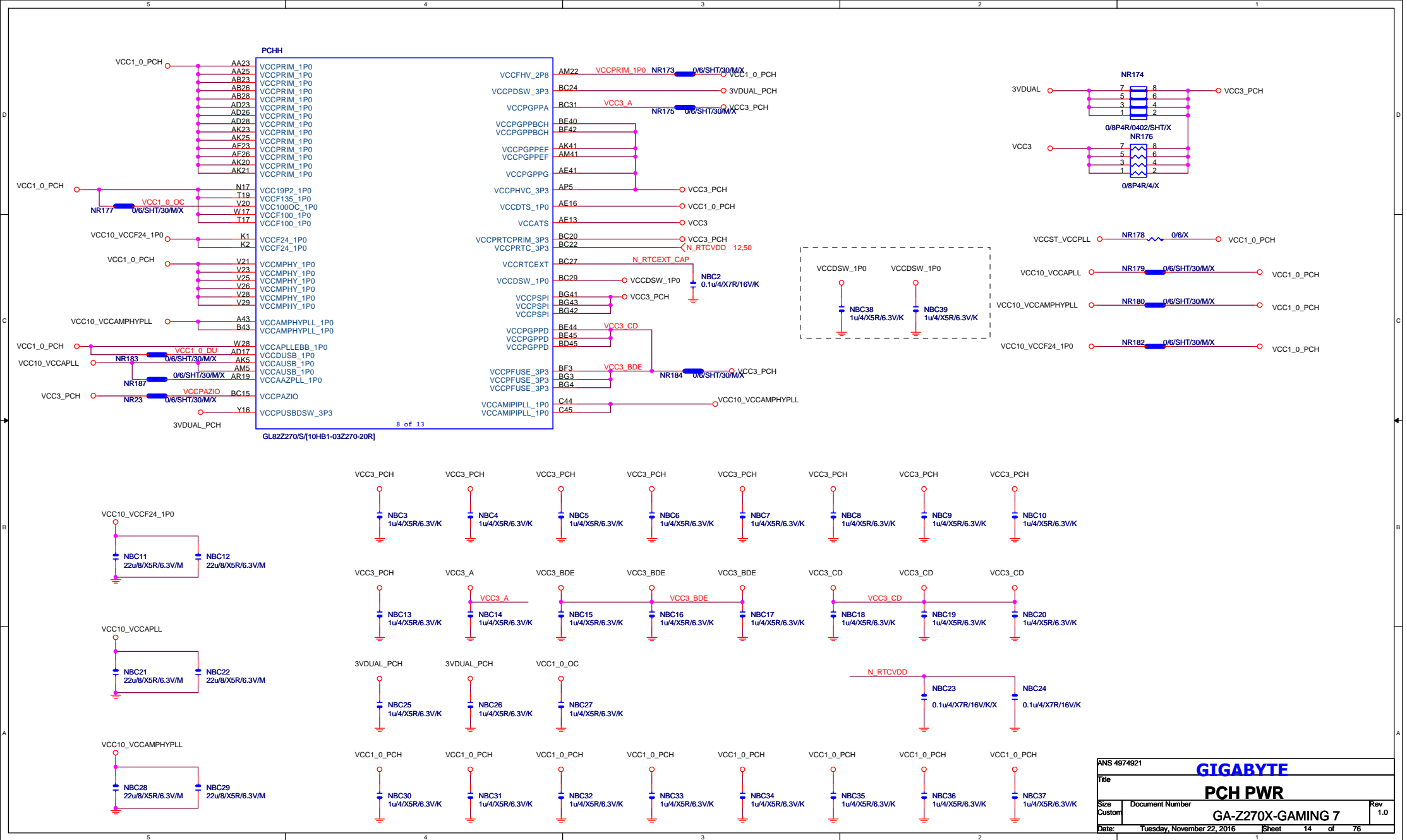














PCHI		
A25	VSS	
A30	VSS	
P22	VSS	
AV38	VSS	
AV45	VSS	
AV8	VSS	
AY11	VSS	
AY19	VSS	
AY37	VSS	
AY4	VSS	
AY42	VSS	
AY8	VSS	
B25	VSS	
B3	VSS	
B30	VSS	
B35	VSS	
B4	VSS	
B41	VSS	
BA13	VSS	
BA17	VSS	
BA29	VSS	
BA31	VSS	
BA37	VSS	
BA4	VSS	
BA42	VSS	
BA40	VSS	
BC38	VSS	
BC40	VSS	
BC9	VSS	
BD11	VSS	
BD16	VSS	
BD2	VSS	
BD21	VSS	
BD25	VSS	
F2	VSS	
E31	VSS	
E6	VSS	
F8	VSS	
F39	VSS	
F43	VSS	
G4	VSS	
G40	VSS	
G42	VSS	
F6	VSS	
G9	VSS	
H11	VSS	
H13	VSS	
H17	VSS	
H19	VSS	
H22	VSS	
H24	VSS	
H27	VSS	
H29	VSS	
H33	VSS	
H35	VSS	
H38	VSS	
H4	VSS	
H42	VSS	
H9	VSS	
J4	VSS	
M36	VSS	
M38	VSS	
M4	VSS	
M8	VSS	
M9	VSS	
N13	VSS	
N15	VSS	
N19	VSS	
N22	VSS	
N24	VSS	
N31	VSS	
N42	VSS	
P10	VSS	
P12	VSS	
AV35	VSS	

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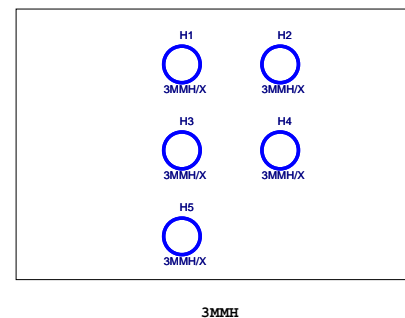
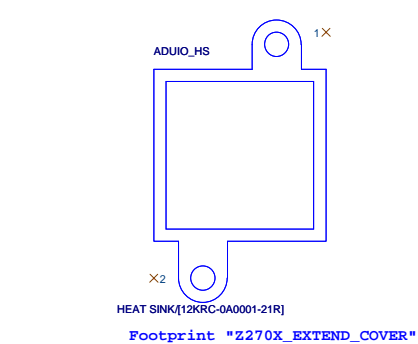
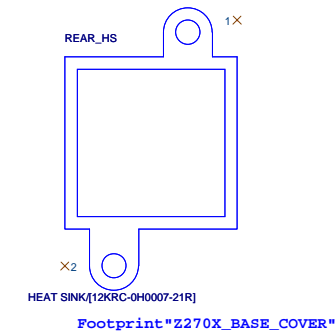
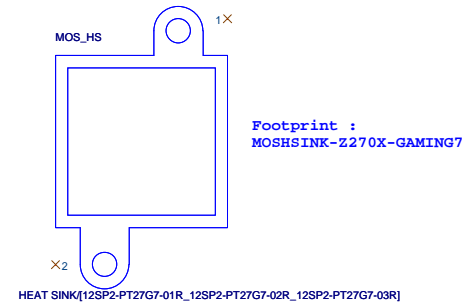
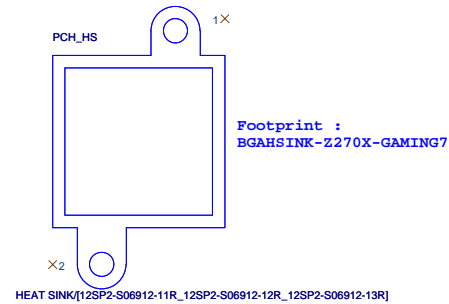
GL82270/S([10HB1-032270-20R])

PCHL		
BD34	VSS[70]	AB18
BD39	VSS[71]	AB20
BD7	VSS[72]	AB21
BE2	VSS[73]	AB25
BF43	VSS[74]	AB29
BF5	VSS[75]	AB4
BG18	VSS[76]	AB42
BG23	VSS[77]	AC10
BG28	VSS[78]	AC11
BG32	VSS[78]	AC14
BG37	VSS[80]	AC16
BG40	VSS[81]	AC38
BG9	VSS[83]	AC4
C1	VSS[84]	AC5
A12	VSS[85]	AC7
C2	VSS[86]	AC8
C37	VSS[87]	AD1
A6	VSS[88]	AD18
C9	VSS[89]	AD20
D1	VSS[90]	AD21
AE8	VSS[92]	AD25
AF18	VSS[93]	AD29
AF20	VSS[94]	AD45
AF21	VSS[94]	AE11
AF25	VSS[95]	AE14
AF28	VSS[96]	AE32
AF29	VSS[96]	AE33
AF4	VSS[98]	AE38
AF42	VSS[99]	AK29
AG18	VSS[100]	AK30
AG20	VSS[101]	AK32
AG21	VSS[102]	AK35
AG23	VSS[103]	AK39
AG25	VSS[104]	AL4
AG26	VSS[105]	AL42
AG28	VSS[106]	AM10
D7	VSS[107]	AM11
P13	VSS[108]	AM13
P15	VSS[109]	AM17
P17	VSS[110]	AM19
P19	VSS[111]	AM24
P21	VSS[112]	AM27
P33	VSS[113]	AM29
P35	VSS[114]	AM32
P4	VSS[115]	AM33
P42	VSS[116]	AM4
P8	VSS[117]	AN45
R1	VSS[118]	AP10
R32	VSS[119]	AP11
T10	VSS[120]	AP13
T14	VSS[121]	AP15
T22	VSS[122]	AP22
T29	VSS[123]	AP27
T32	VSS[124]	AP31
T36	VSS[125]	AP33
T38	VSS[126]	AP34
Y38	VSS[127]	AP39
Y4	VSS[128]	T4
Y8	VSS[129]	W26
T42	VSS[130]	V16
T5	VSS[131]	V17
U4	VSS[132]	V18
U42	VSS[133]	V30
V10	VSS[134]	V32
V14	VSS[135]	V33
W3	VSS[136]	V38
AR13	VSS[137]	V4
AR31	VSS[138]	V8
AR33	VSS[139]	W18
AR4	VSS[140]	W20
AT10	VSS[141]	W21
AT13	VSS[142]	W23
AT35	VSS[143]	W25
AT37	VSS[144]	
AT42	VSS[145]	
AU11	VSS[146]	A44
AU17	VSS[147]	BE1
BD30	VSS[148]	BD1
W45	VSS[149]	B1
Y13	VSS[150]	A2
Y14	VSS[151]	B2
Y30	VSS[152]	A3
Y32	VSS[153]	A4
Y33	VSS[154]	B44
BG14	VSS[155]	B45
VSS_BG14	VSS[156]	

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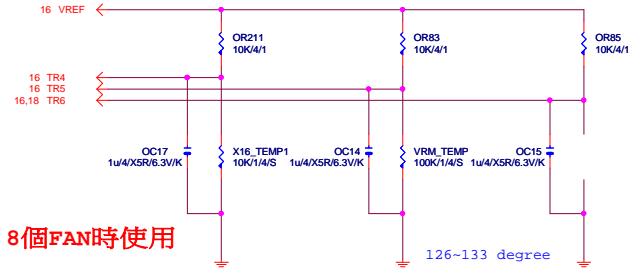
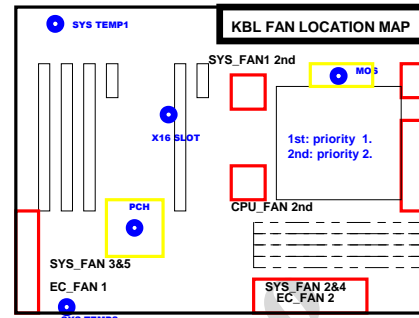
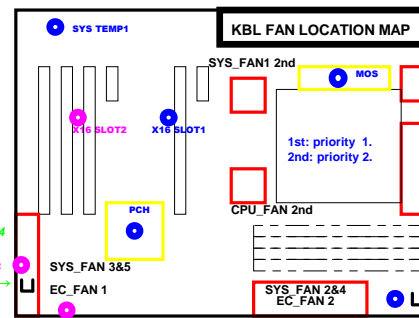
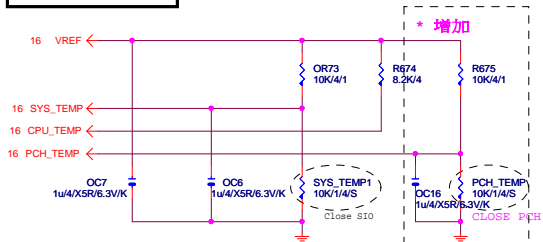
GL82270/S([10HB1-032270-20R])

## 装甲HEATSINK 分成四大部份

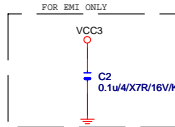
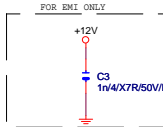
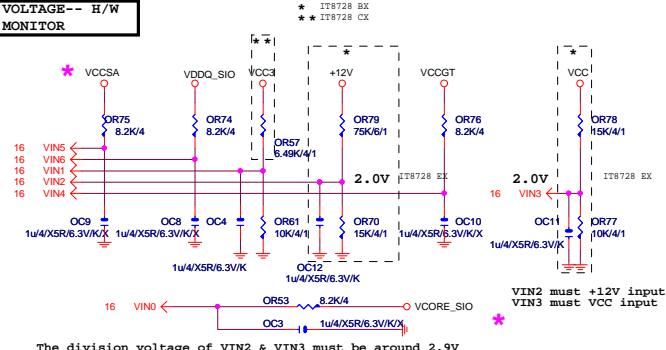




# TEMP H/W MONITOR



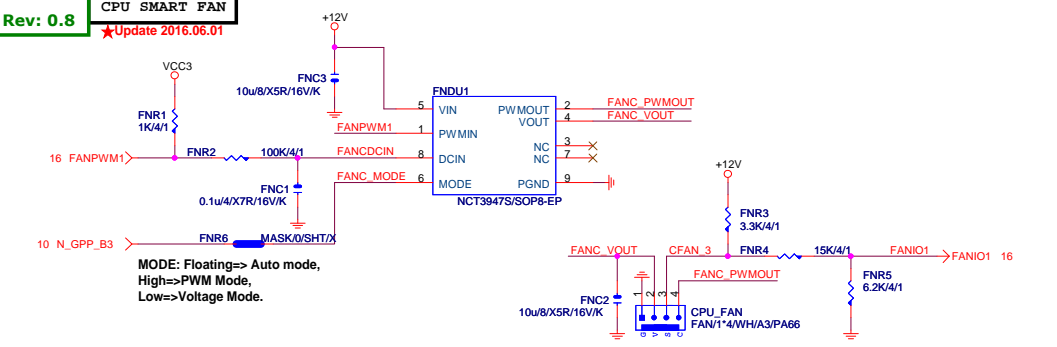
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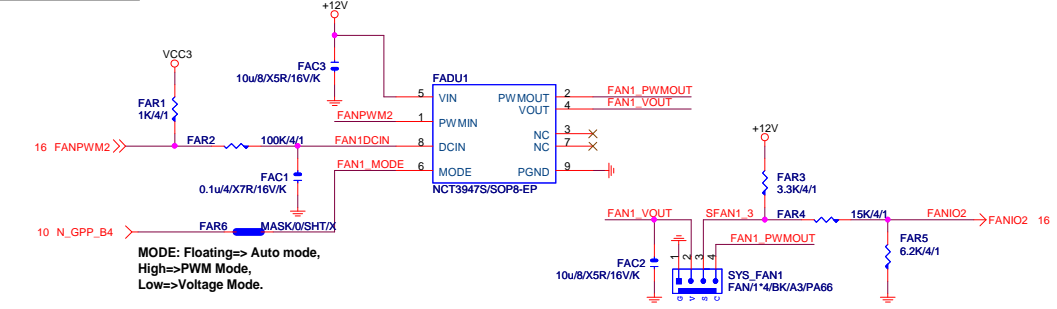
★Update 2015-04.24

Gigabyte Technology

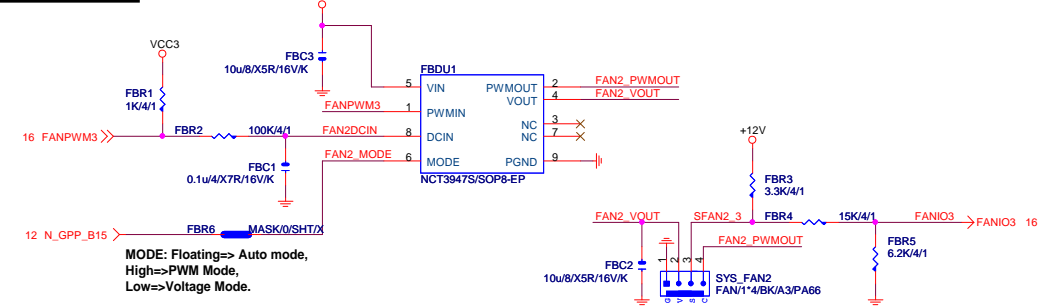
Title			HWM,KB/MS, FAN CTRL
Size	Document Number		
Custom		GA-Z270X-GAMING 7	
Date:	Tuesday, November 22, 2016	Sheet	17 of 76
			Rev 1.0



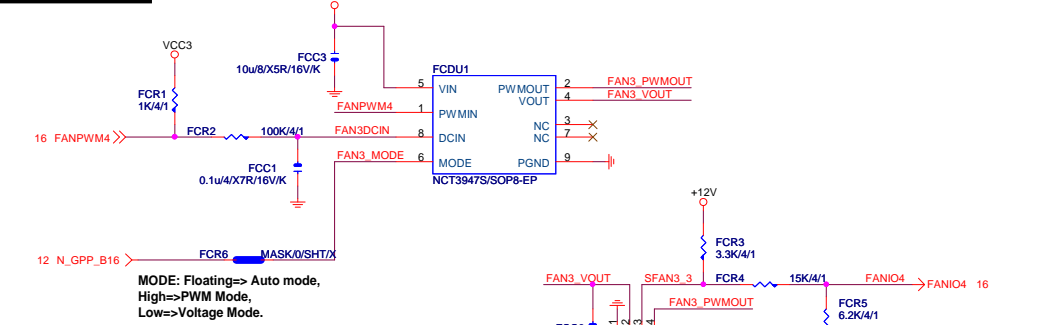
SYSTEM FAN1



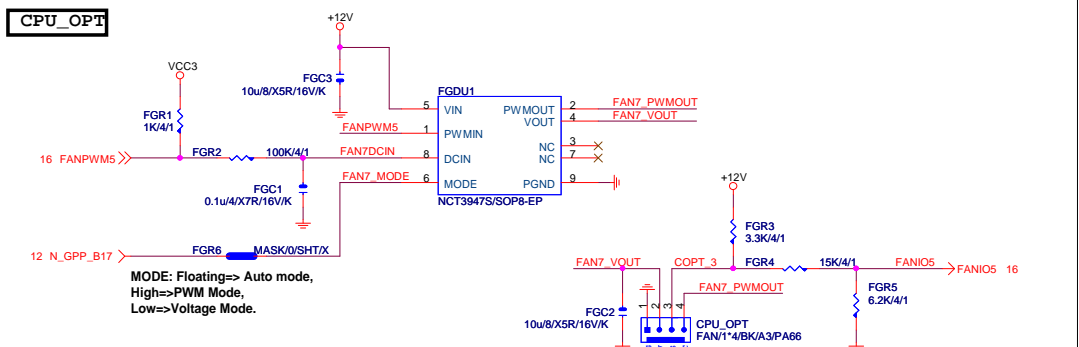
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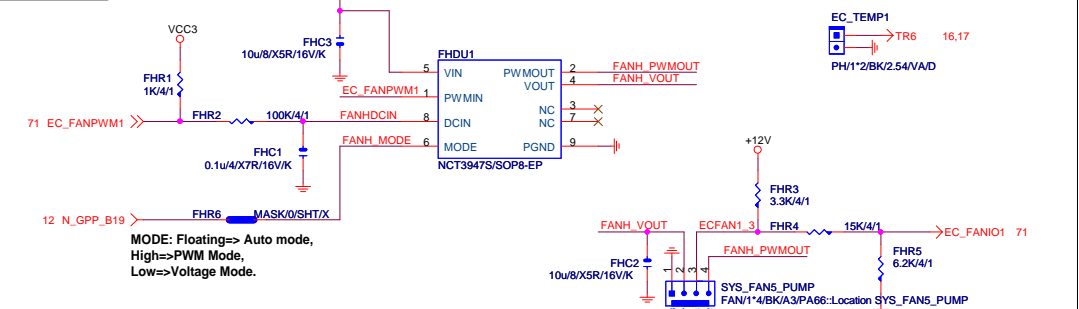
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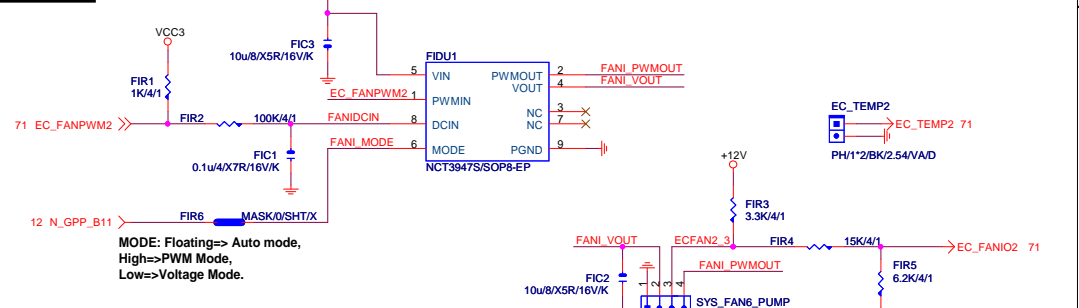
CPU\_OPT



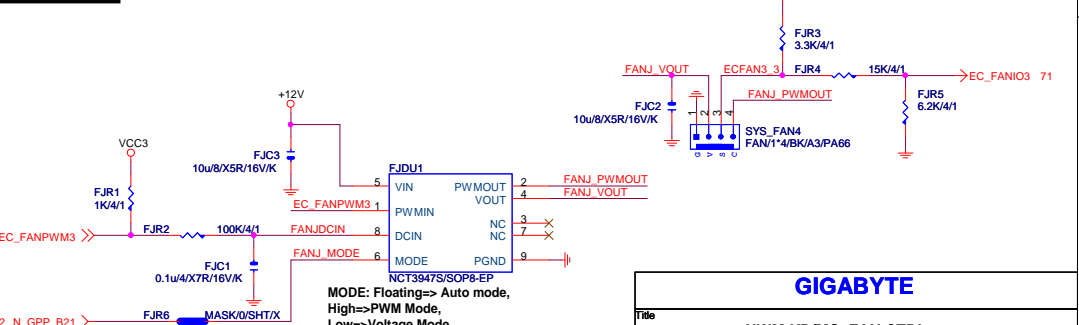
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CPU\_PUMP2

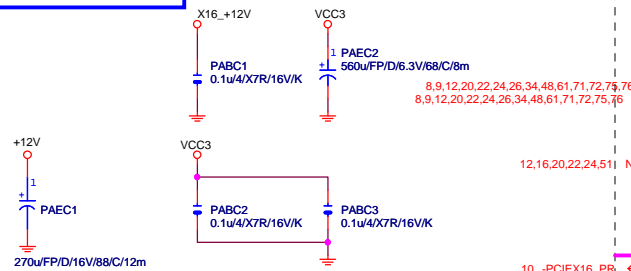


SYSTEM\_FAN4



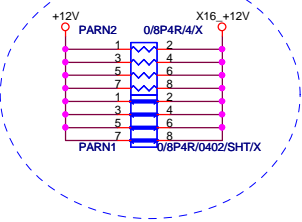
KBL FAN LOCATION MAP REFER TO PAGE.27

## PCIESLOT-164STH



## PCIEX16 PROTECT SHT

```
+12 protect
short-wire test
```



PCIEX16	AC	CAP
---------	----	-----

PA EXP TXPO	PA05	0.22uX4XSR/6.3V/K	PA EXP TXPO C
PA EXP TXN0	PA04	0.22uX4XSR/6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PA06	0.22uX4XSR/6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PA07	0.22uX4XSR/6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PA08	0.22uX4XSR/6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PA09	0.22uX4XSR/6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PA10	0.22uX4XSR/6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PA11	0.22uX4XSR/6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PA12	0.22uX4XSR/6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PA13	0.22uX4XSR/6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PA14	0.22uX4XSR/6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PA15	0.22uX4XSR/6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PA16	0.22uX4XSR/6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PA17	0.22uX4XSR/6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PA18	0.22uX4XSR/6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PA19	0.22uX4XSR/6.3V/K	PA EXP TXN7 C
PA EXP SW TPX8	PA21	0.22uX4XSR/6.3V/K	PA EXP SW TPX8 C
PA EXP SW TXN8	PA20	0.22uX4XSR/6.3V/K	PA EXP SW TXN8 C
PA EXP SW TPX9	PA22	0.22uX4XSR/6.3V/K	PA EXP SW TPX9 C
PA EXP SW TXN9	PA23	0.22uX4XSR/6.3V/K	PA EXP SW TXN9 C
PA EXP SW TPX10	PA24	0.22uX4XSR/6.3V/K	PA EXP SW TPX10 C
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PA EXP SW TPX11	PA26	0.22uX4XSR/6.3V/K	PA EXP SW TPX11 C
PA EXP SW TXN11	PA27	0.22uX4XSR/6.3V/K	PA EXP SW TXN11 C
PA EXP SW TPX12	PA28	0.22uX4XSR/6.3V/K	PA EXP SW TPX12 C
PA EXP SW TXN12	PA29	0.22uX4XSR/6.3V/K	PA EXP SW TXN12 C
PA EXP SW TPX13	PA30	0.22uX4XSR/6.3V/K	PA EXP SW TPX13 C
PA EXP SW TXN13	PA31	0.22uX4XSR/6.3V/K	PA EXP SW TXN13 C
PA EXP SW TPX14	PA32	0.22uX4XSR/6.3V/K	PA EXP SW TPX14 C
PA EXP SW TXN14	PA33	0.22uX4XSR/6.3V/K	PA EXP SW TXN14 C
PA EXP SW TPX15	PA34	0.22uX4XSR/6.3V/K	PA EXP SW TPX15 C
PA EXP SW TXN15	PA35	0.22uX4XSR/6.3V/K	PA EXP SW TXN15 C

PCI-E REV:1.1--&gt; 2.5GHZ

PCE-E X1(單向) BANDWIDTH=2.5GHz\*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWIDTH=2.5GHz\*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWIDTH=2.5GHz\*(8b/10b)X16=32Gb/s=4GB/s

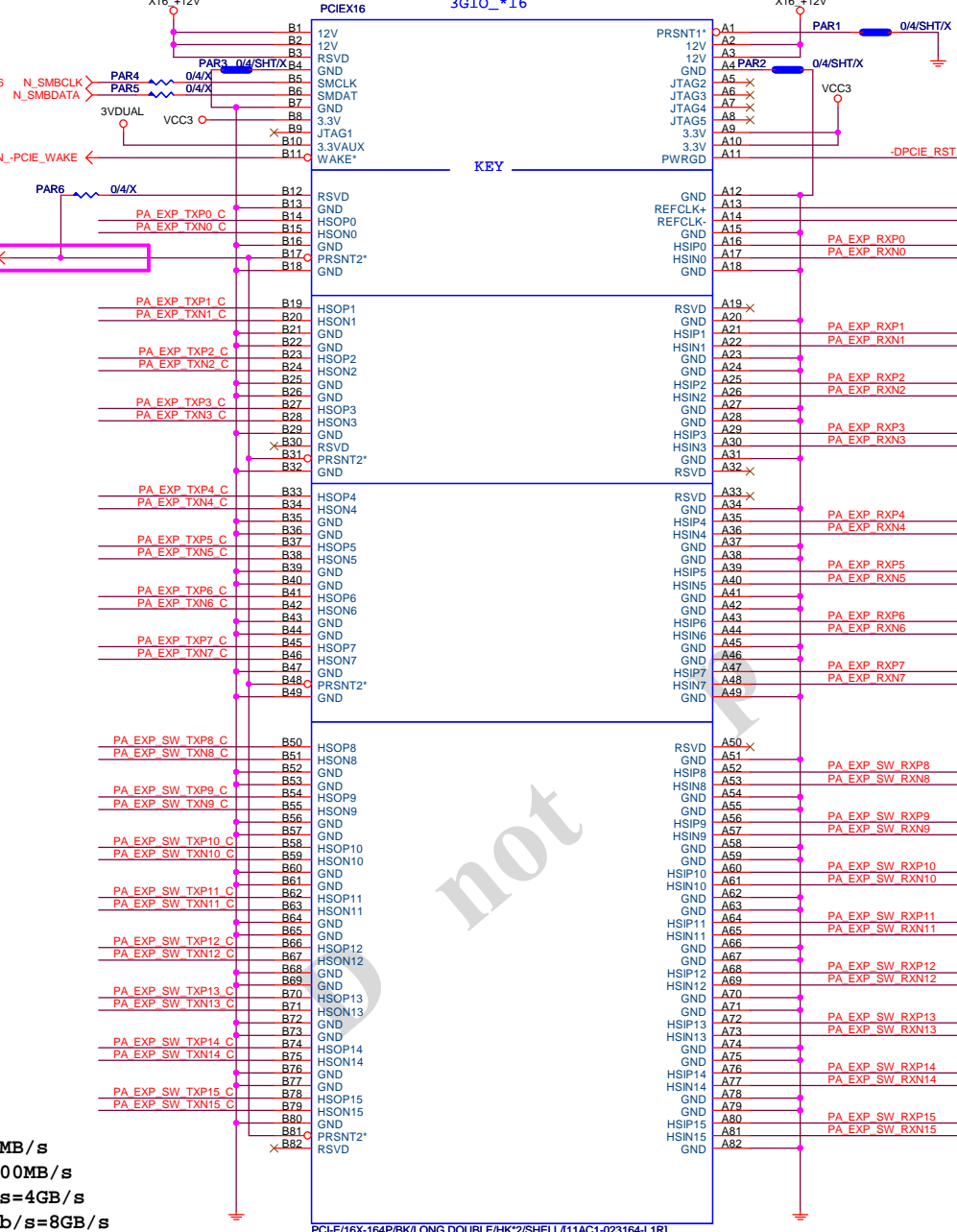
PCE-E X16(雙向) BANDWITH=2.5GHz\*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--&gt; 5GHZ

PCE-E X1(單向) BANDWIDTH=5GHz\*(8b/10b)=4Gb/s=500MB/s

PCI-E REV:3.0--&gt; 8GHZ

PCE-E X1(單向) BANDWITH=8GHz\*(128b/130b)=8Gb/s=1GB/s

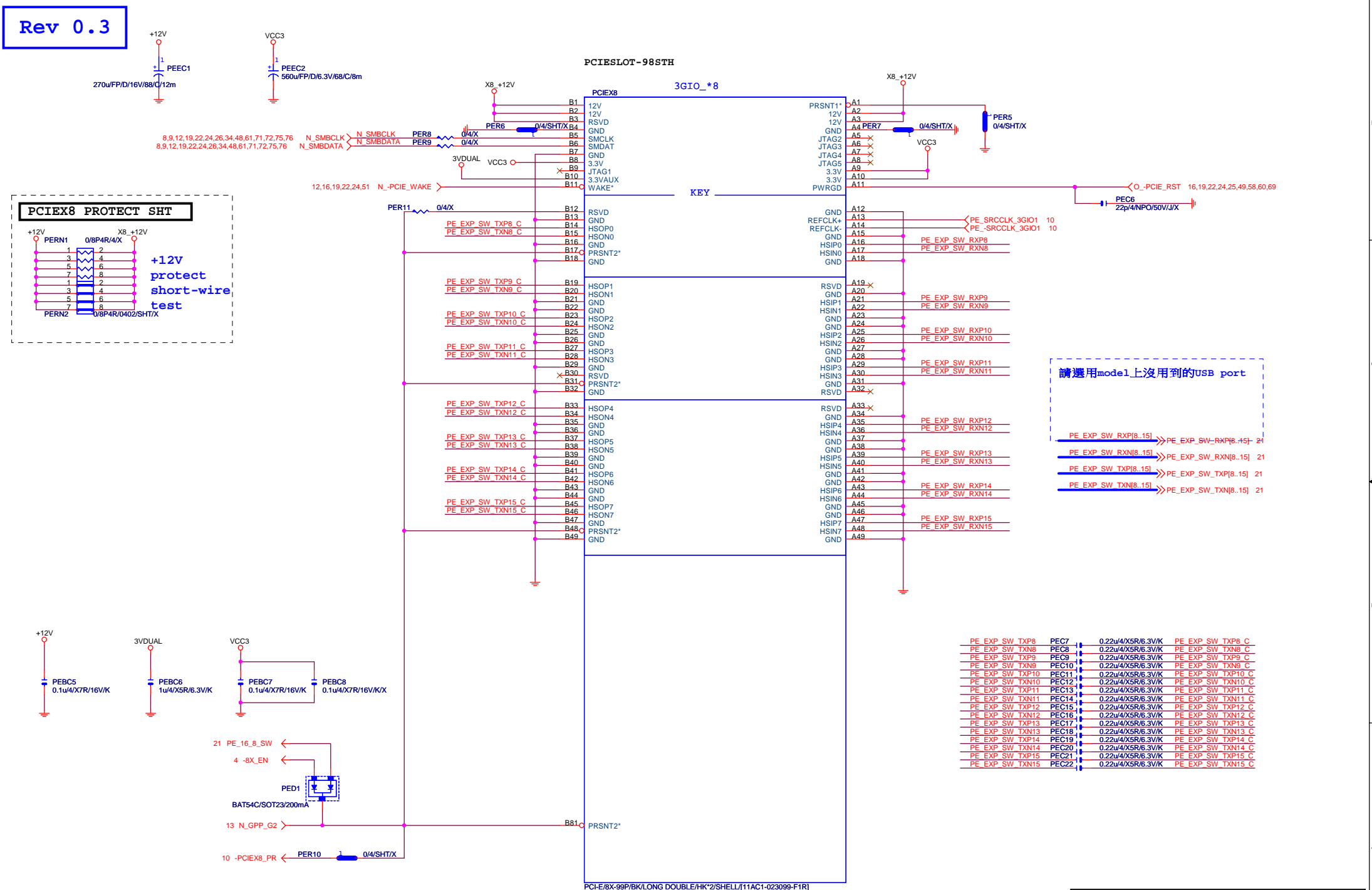
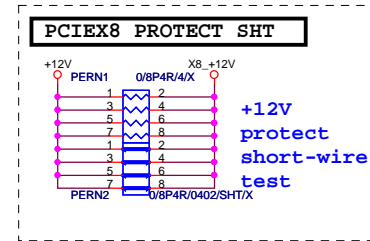
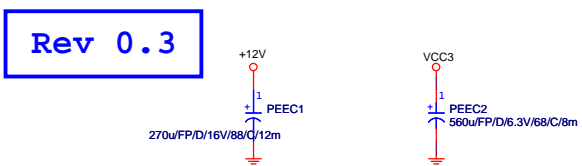


## PCIEX16:16/5/5/5/16

<u>PA_EXP_RXP[0..15]</u>	»»PA_EXP_RXP[0..15]	4,21
<u>PA_EXP_RXN[0..15]</u>	»»PA_EXP_RXN[0..15]	4,21
<u>PA_EXP_TXP[0..15]</u>	»»PA_EXP_TXP[0..15]	4,21
<u>PA_EXP_TXN[0..15]</u>	»»PA_EXP_TXN[0..15]	4,21
<u>PA_EXP_SW_RXP[8..15]</u>	»»PA_EXP_SW_RXP[8..15]	21
<u>PA_EXP_SW_RXN[8..15]</u>	»»PA_EXP_SW_RXN[8..15]	21
<u>PA_EXP_SW_TXP[8..15]</u>	»»PA_EXP_SW_TXP[8..15]	21
<u>PA_EXP_SW_TXN[8..15]</u>	»»PA_EXP_SW_TXN[8..15]	21

## 黑色金屬加強

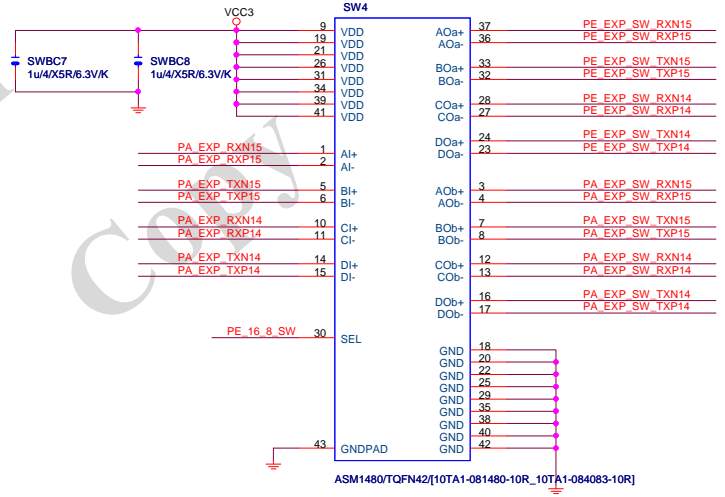
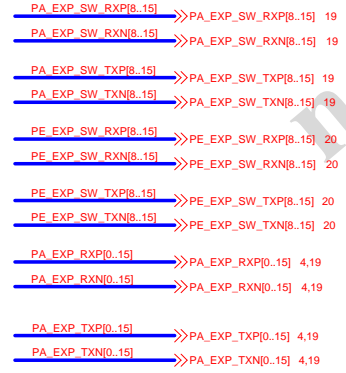
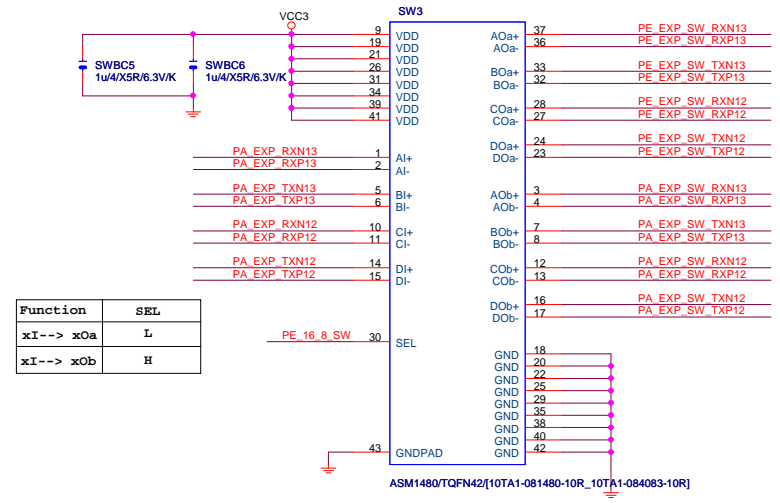
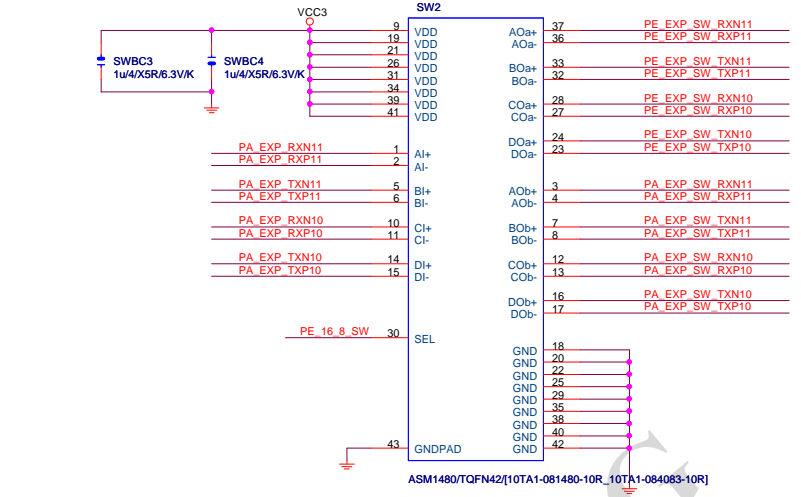
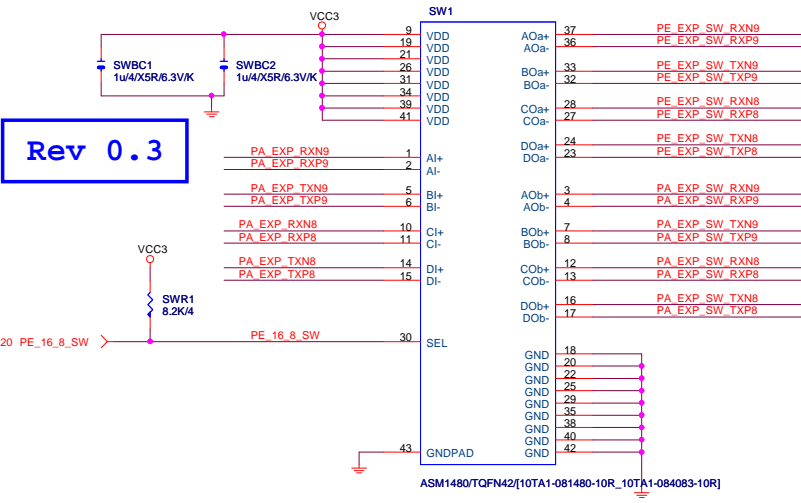
Rev 0.3



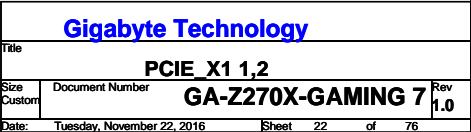
## 黑色金屬加強



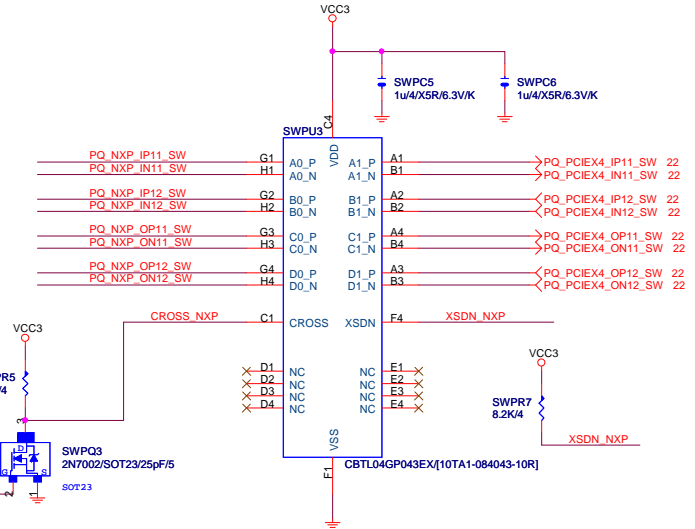
Rev 0.3



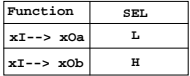
Function	SEL
xI--> x0a	L
xI--> x0b	H



Rev 0.1

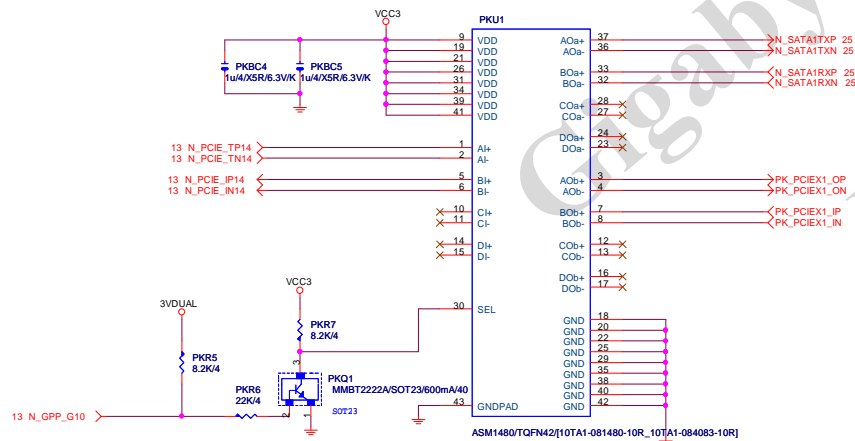
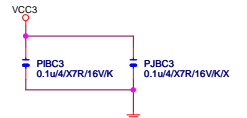
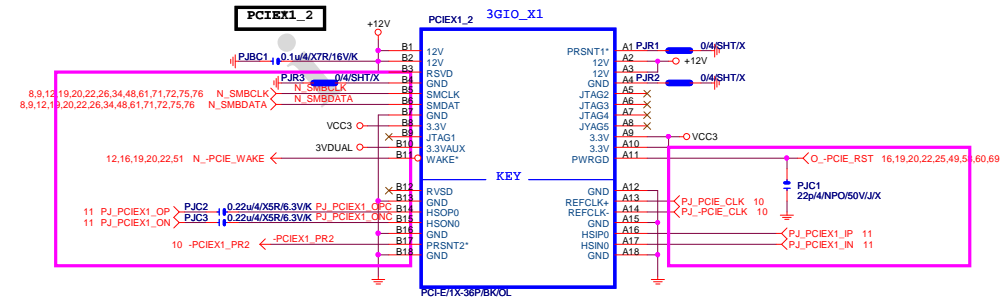
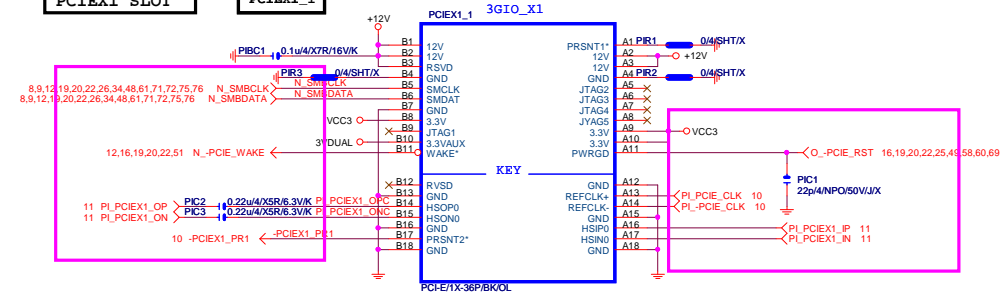


Flex IO priority	N_GPP_G0 (PCH_GPP_G0)	N_GPP_D16 (PCH_GPP_D16)
M2P_32G Only	L	H
PCIEX4 Only (PCIe Reverse)	H	L
M2P_32G + PCIEX4 (M2P_32Gx2+PCIEX4_x2)	L	L

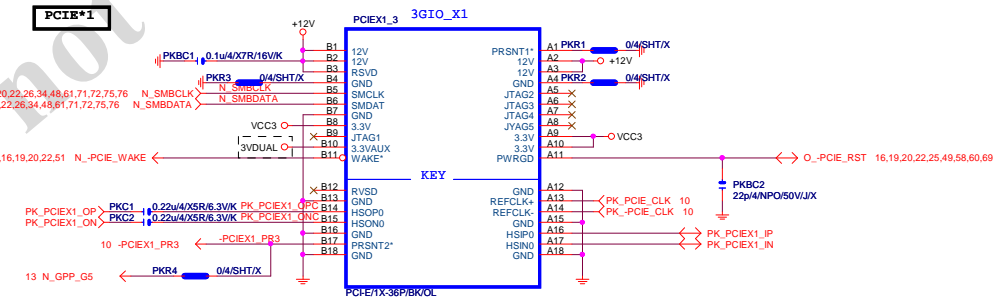


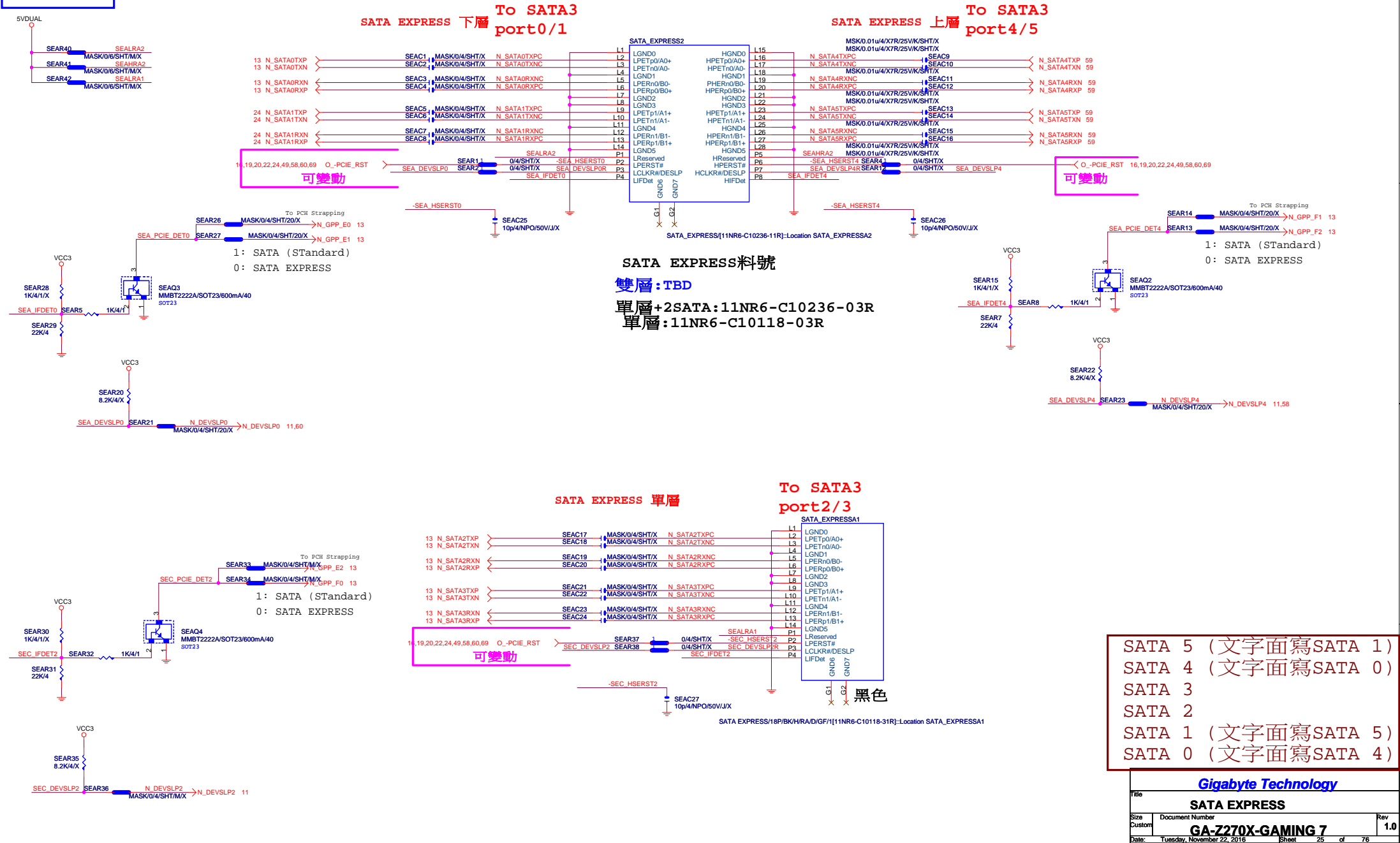
	N_GPP_G3 (PCH GPP_G3)	N_GPP_G4 (PCH GPP_G4)	N_GPP_G9 (PCH GPP_G9)
→	H	H	H
→	L	L	H
→	H	L	L

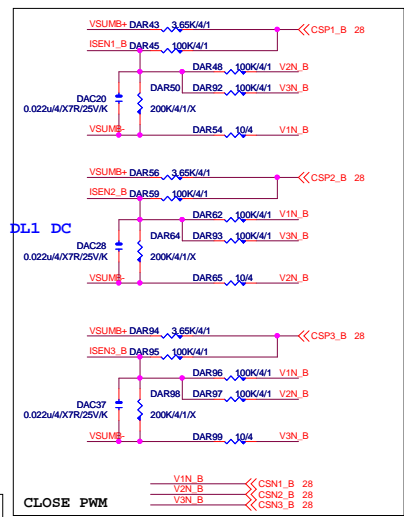
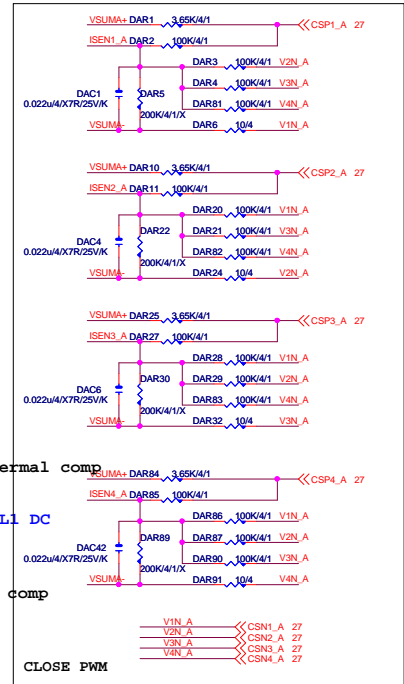
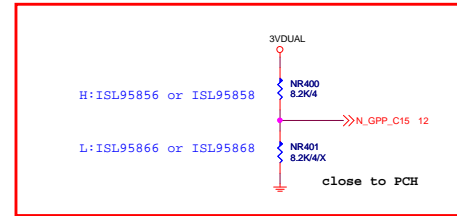
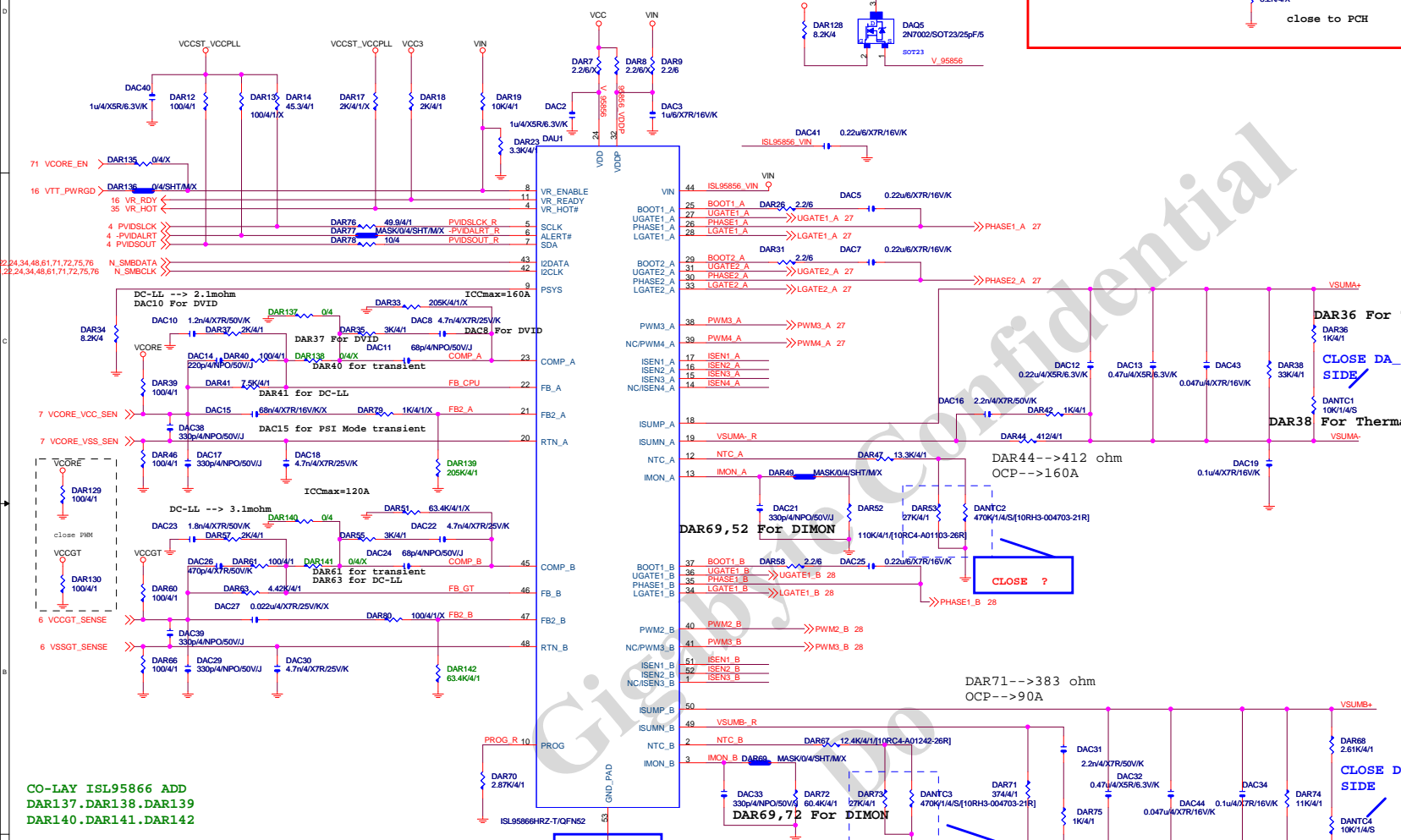
<p align="center"><b>Gigabyte Technology</b></p> <p align="center"><b>SWITCH</b></p>			
Title			
Size	Document Number		Rev
Custom	<b>GA-Z270X-GAMING 7</b>		<b>1.0</b>
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Function	SEL
xI--> x0a	L
xI--> x0b	H





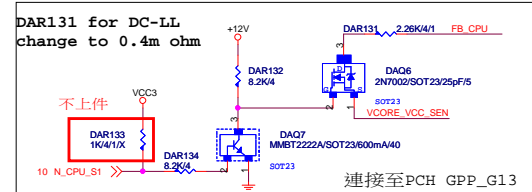
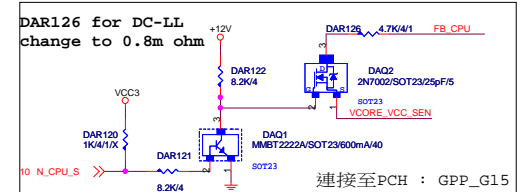
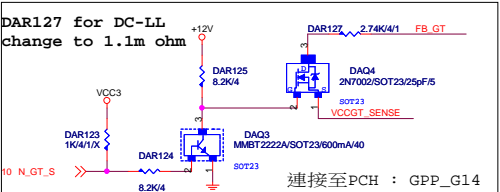


CO-LAY ISL95866 ADD  
DAR137.DAR138.DAR139  
DAR140.DAR141.DAR142

VCORE	ISL95856	ISL95866	VCCGT	ISL95856	ISL95866
DAR137	X	V	DAR140	X	V
DAR138	V	X	DAR141	V	X
DAR139	X	V	DAR142	X	V
DAC15	V	X	DAC27	V	X
DAR79	V	X	DAR80	V	X
DAR33	V	X	DAR51	V	X

VAXG Loadline	N_GPP_G14
Auto	High
Standard	High
High	Lo

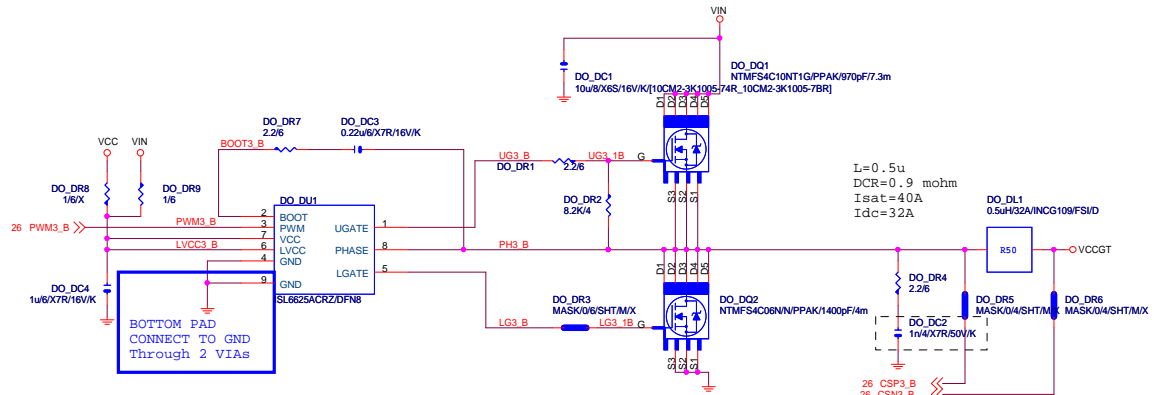
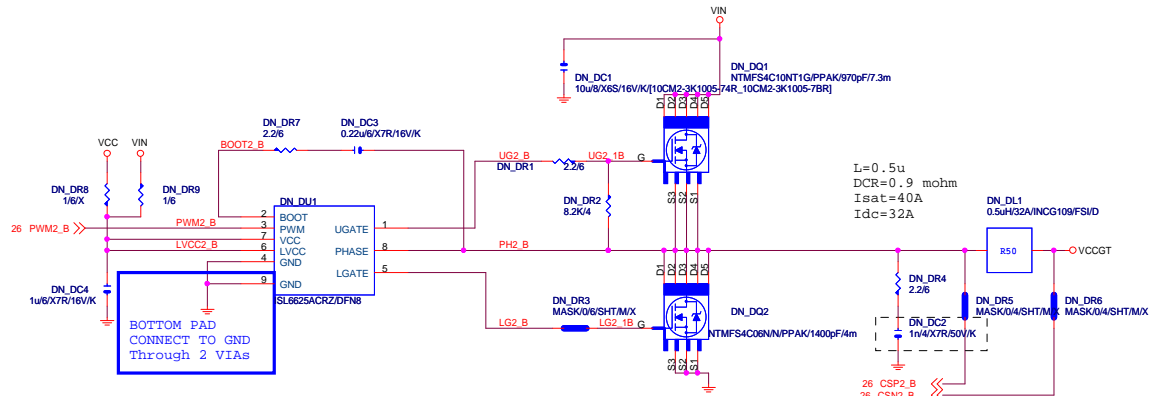
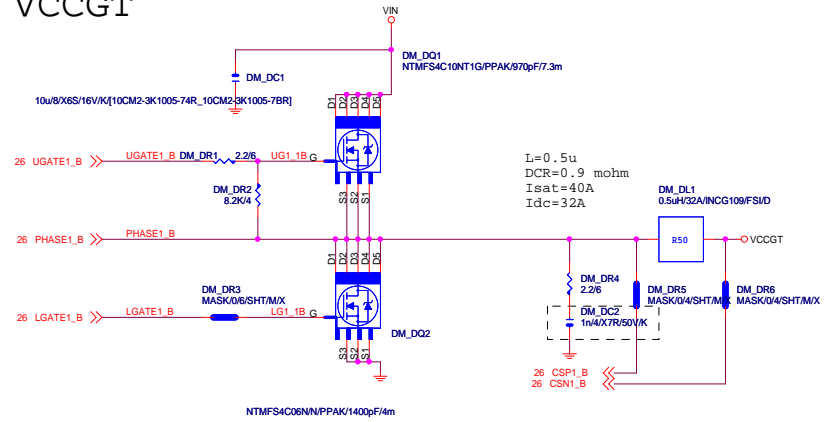
Vcore Loadline	N_GPP_G15	N_GPP_G13
Auto	High	High
Standard	High	High
High	Lo	High
Turbo	High	Lo



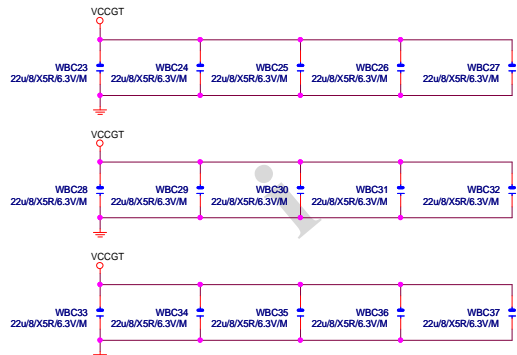
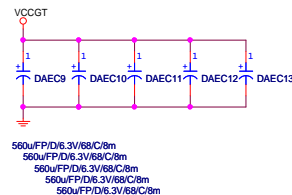




VCCGT



VCCGT CAP 560u\*5PCS  
22u\*15PCS







**VPP 25V**

DDR\_VPP VIN CAP  
560u\*1PCS

2.5V

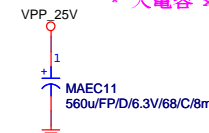
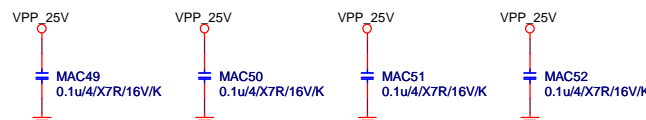
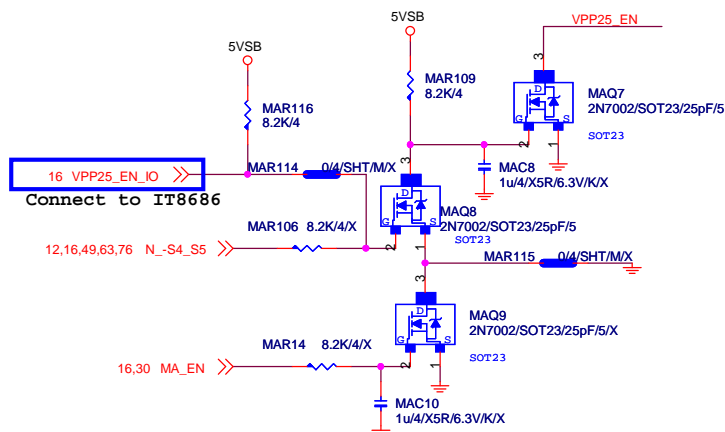


Remote sense請從最重的負載端點拉回

PWR SEQ

VPP CAP 560u\*1PCS

\* 大電容 x1

**GIGABYTE™**

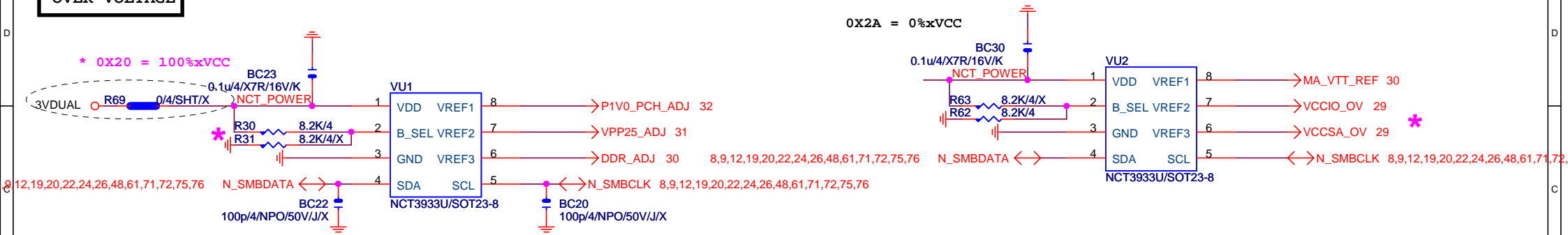
Title			
RT8120_VPP25 POWER			
Size	Document Number	Rev	
Custom	GA-Z270X-GAMING 7	1.0	
Date:	Tuesday, November 22, 2016	Sheet	31 of 76







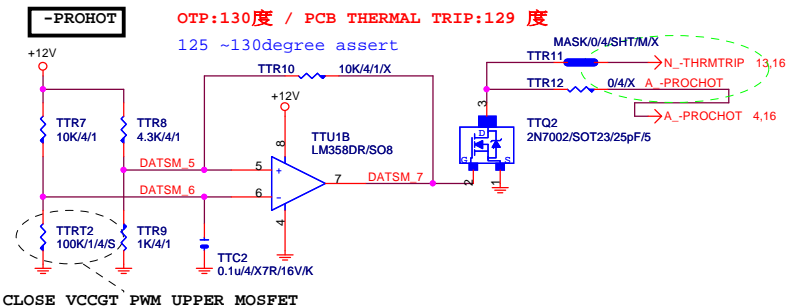
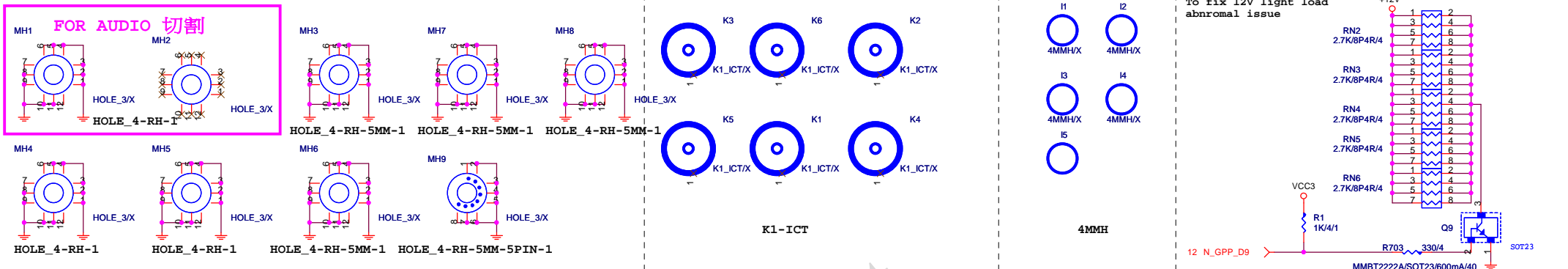
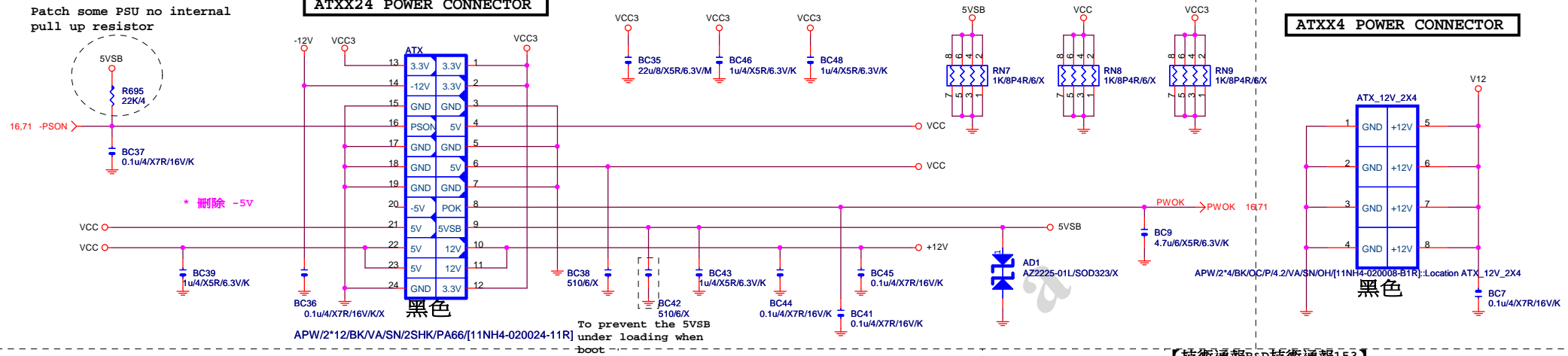
# OVER VOLTAGE

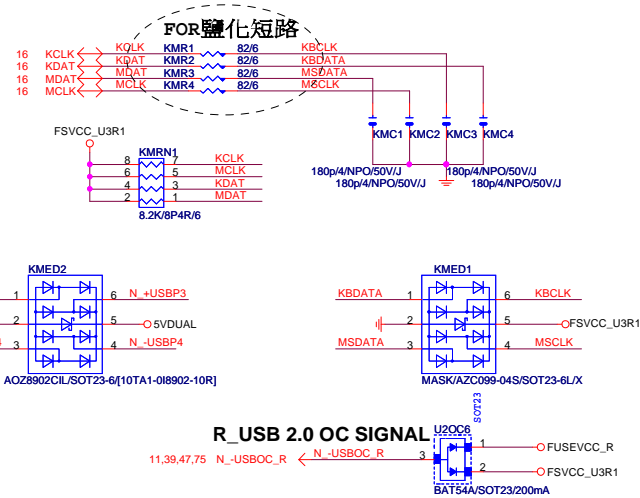


NCT3933	0X2A	0X20	0X22
VREF1	DDRVT	VREF_DDRA_DQ	PCH Core
VREF2	VREF_DDRA_CA	N/A	VCC1_5_PCH
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	SMREF

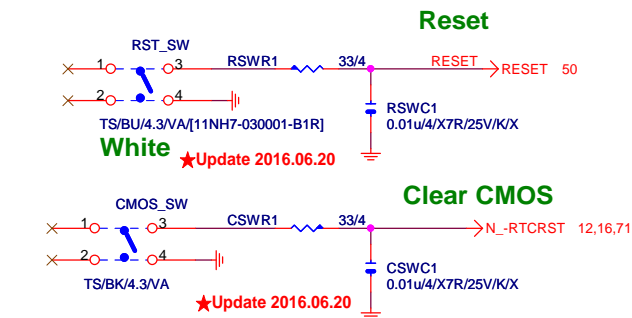
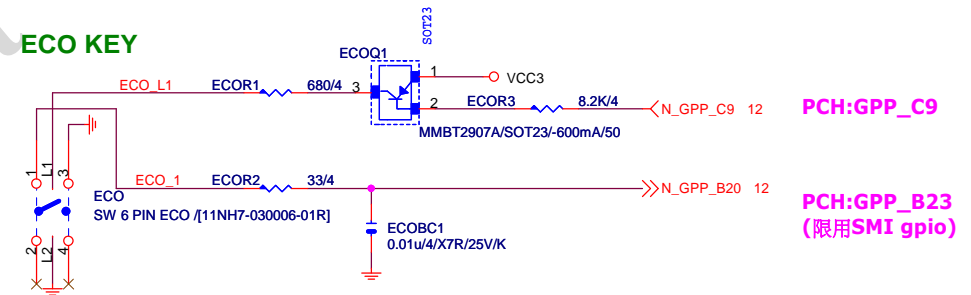
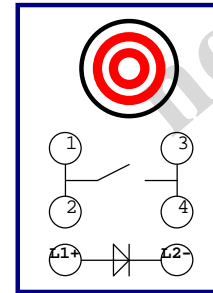
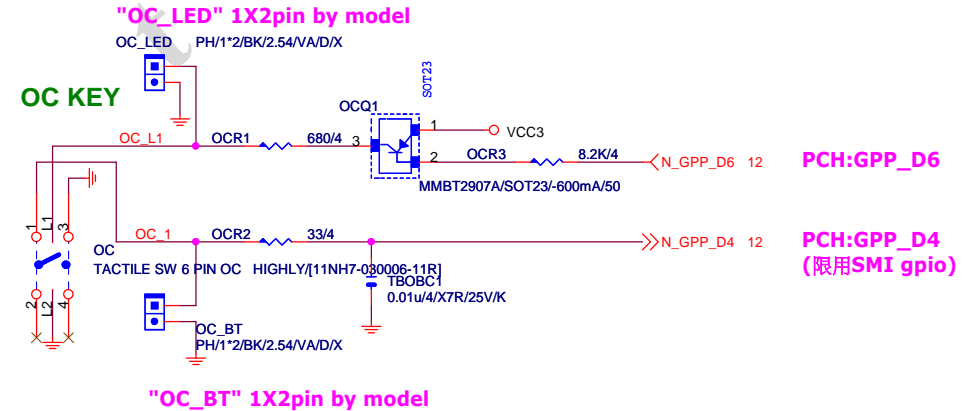
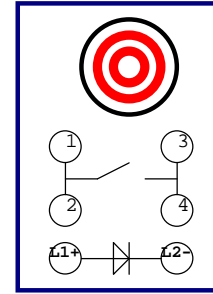
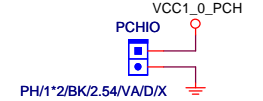
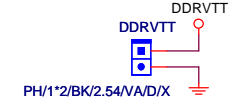
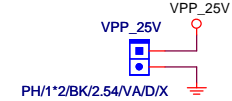
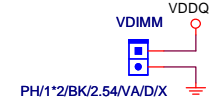
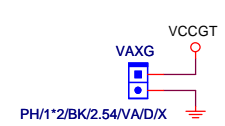
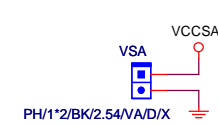
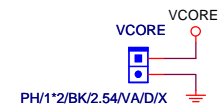
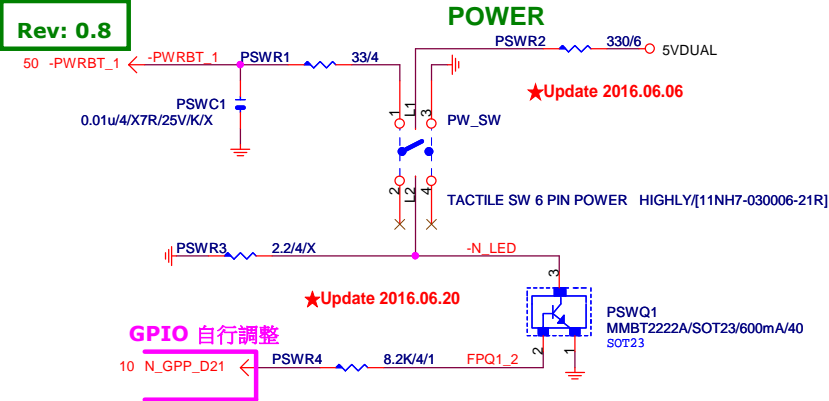
Gigabyte Technology			
CPU CORE VR-2			
Title	GA-Z270X-GAMING 7		
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**ATXX4 POWER CONNECTOR**





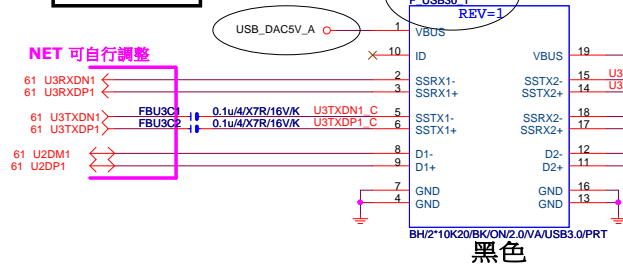
Rev: 0.8



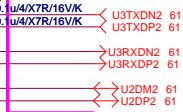
Gigabyte Technology			
Title OC BOTTOM			
Size Custom	Document Number	GA-Z270X-GAMING 7	
Date:	Tuesday, November 22, 2016	Sheet	37 of 76
		1	Rev 1.0

Front USB3.0

NET 可自行調整

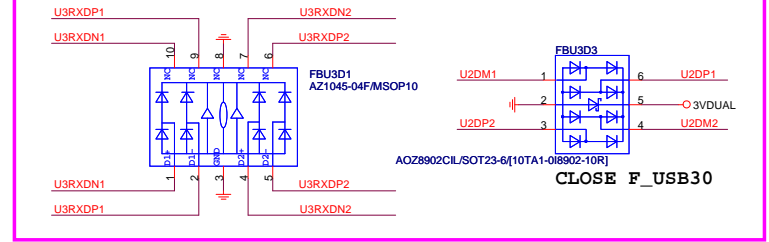


NET 可自行調整



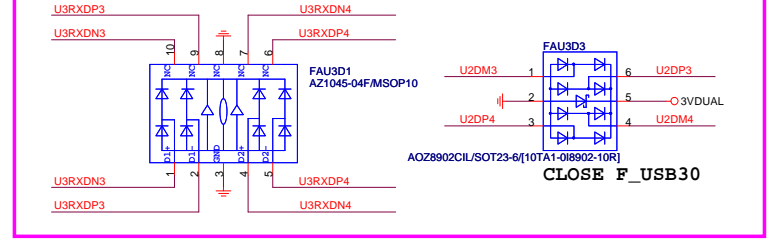
F\_USB POWER PROTECT

NET 可自行調整



CLOSE F\_USB30

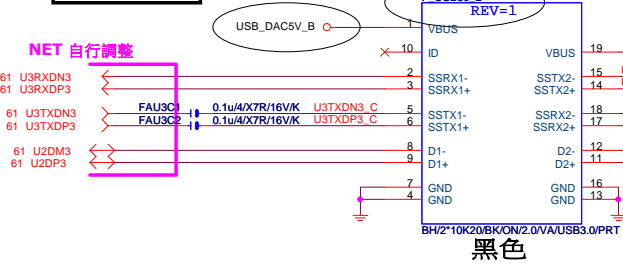
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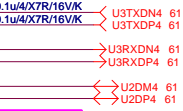
CLOSE F\_USB30

Front USB3.0

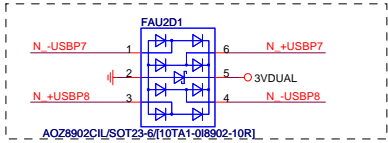
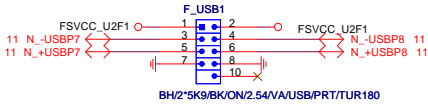
NET 自行調整



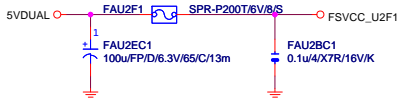
NET 可自行調整



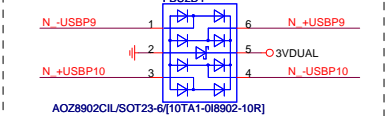
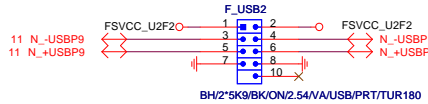
NET 可變



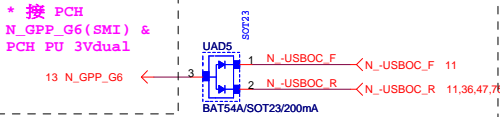
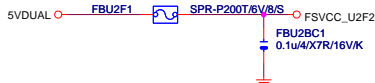
Close to connector  
FUSE 2 Port 1 Fuse 2A



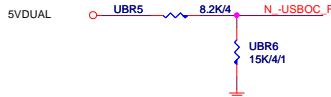
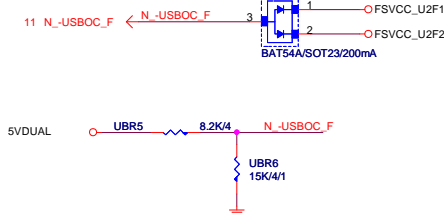
NET 可變



Close to connector  
FUSE 2 Port 1 Fuse 2A

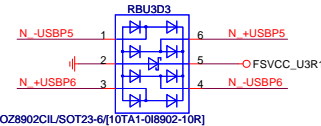
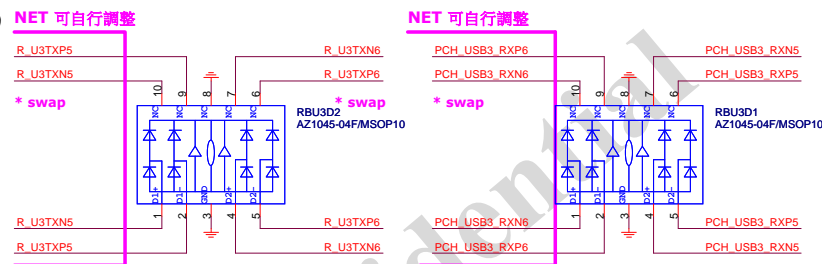
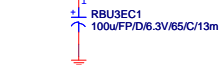


F\_USB 2.0 OC SIGNAL

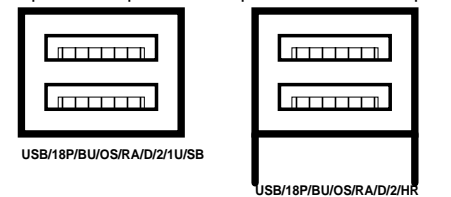




**R USB30**



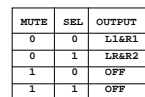
**2 port USB 3.0 Capture:**



**KB\_MS\_USB3, R\_USB30**

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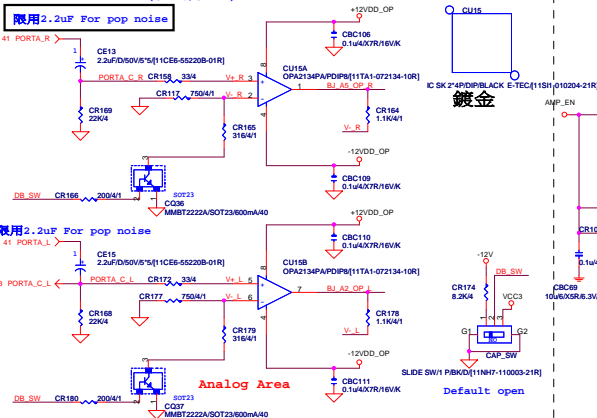
## Rear CTR/SUB &amp; FP HP-Out

MUTE	SEL	OUTPUT
0	0	L1&R1
0	1	LR&R2
1	0	OFF
1	1	OFF

-----  
AMPLIFIED

$$\text{OP AMP. Rate} = (\text{CR118}/\text{CR117})+1$$

限用2.2uF For pop noise



## Line-Out

41 PORTG\_R CE5 2.2uF/D:50V/5%[11CE6-52220B-01R] AJ\_B5\_R AJ\_B5\_R 44  
41 PORTG\_L CE6 2.2uF/D:50V/5%[11CE6-52220B-01R] AJ\_B2\_L AJ\_B2\_L 43.4

限用2.2uF For pop noise

## Rear

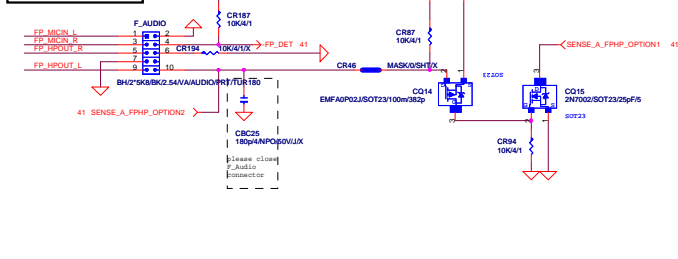
CE14 2.2uF/D50V5%[11CE6-56220B-01R]

41 PORTB\_R > CE16 2.2uF/D50V5%[11CE6-56220B-01R] BJ\_C5\_R > BJ\_C5\_R 44

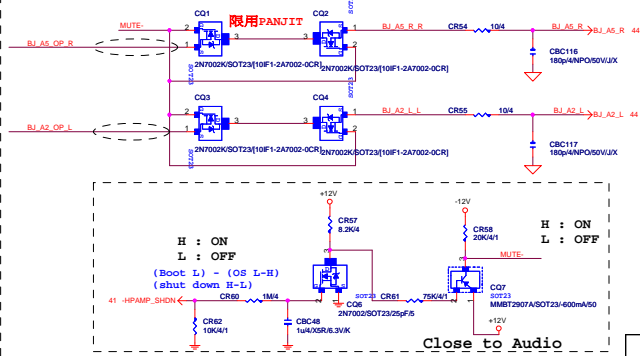
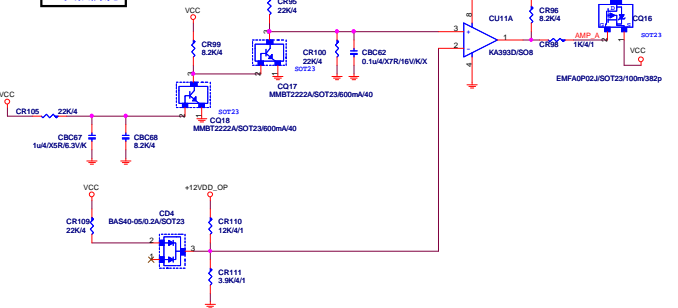
41 PORTB\_L > BJ\_C2\_L > BJ\_C2\_L 44

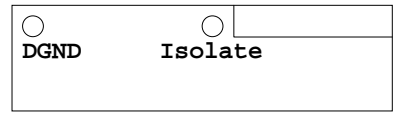
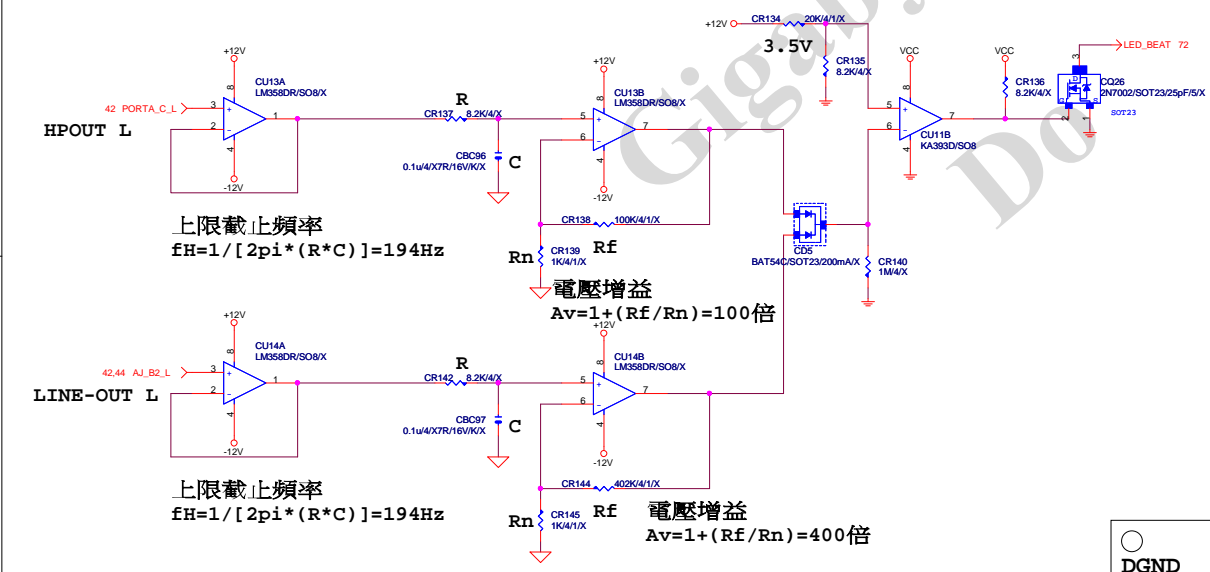
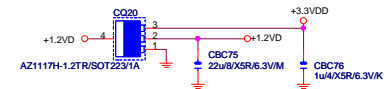
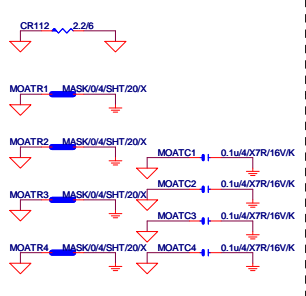
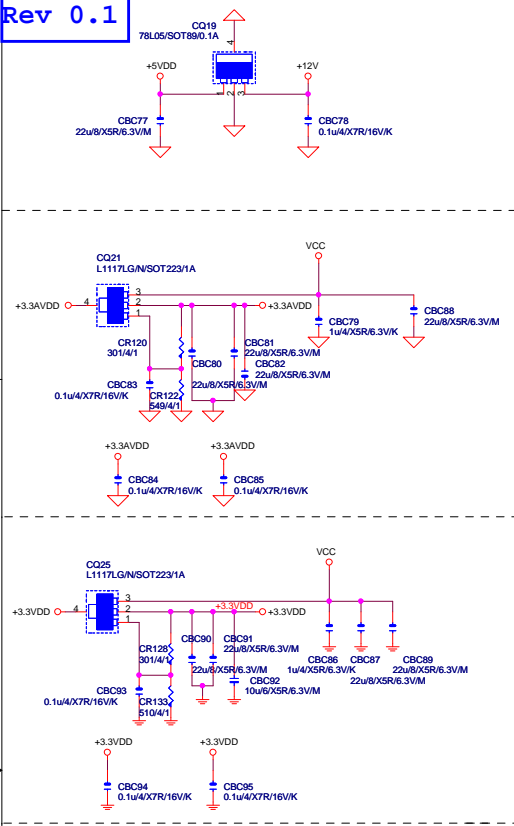
限用2.2uF For pop noise

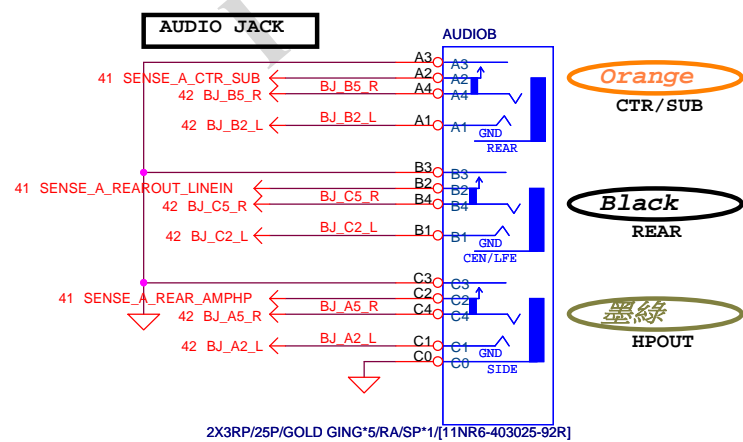
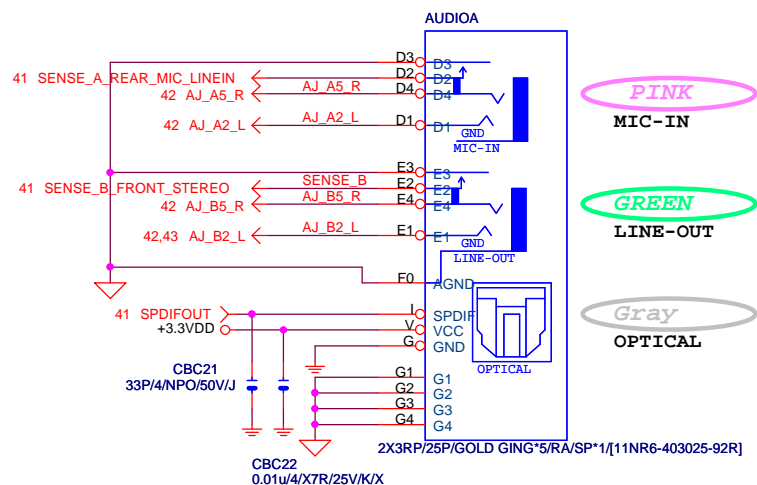
#### HD\_Audio FRONT PANEL



OP反插防燒





**Gigabyte Technology**

Title

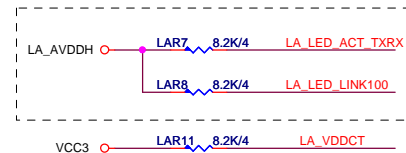
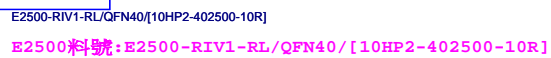
**Creative Sound3Di ZxR**Size  
Custom

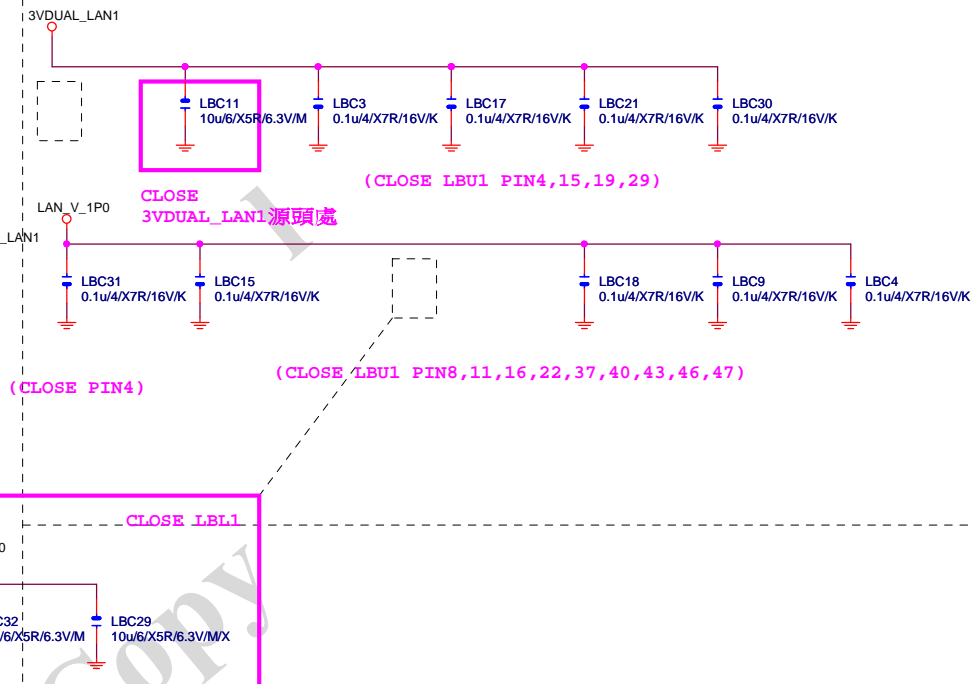
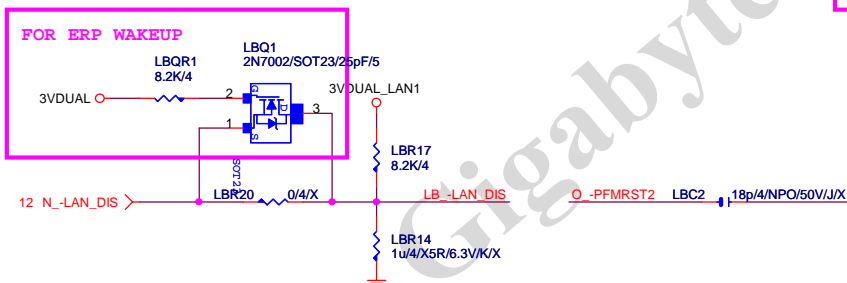
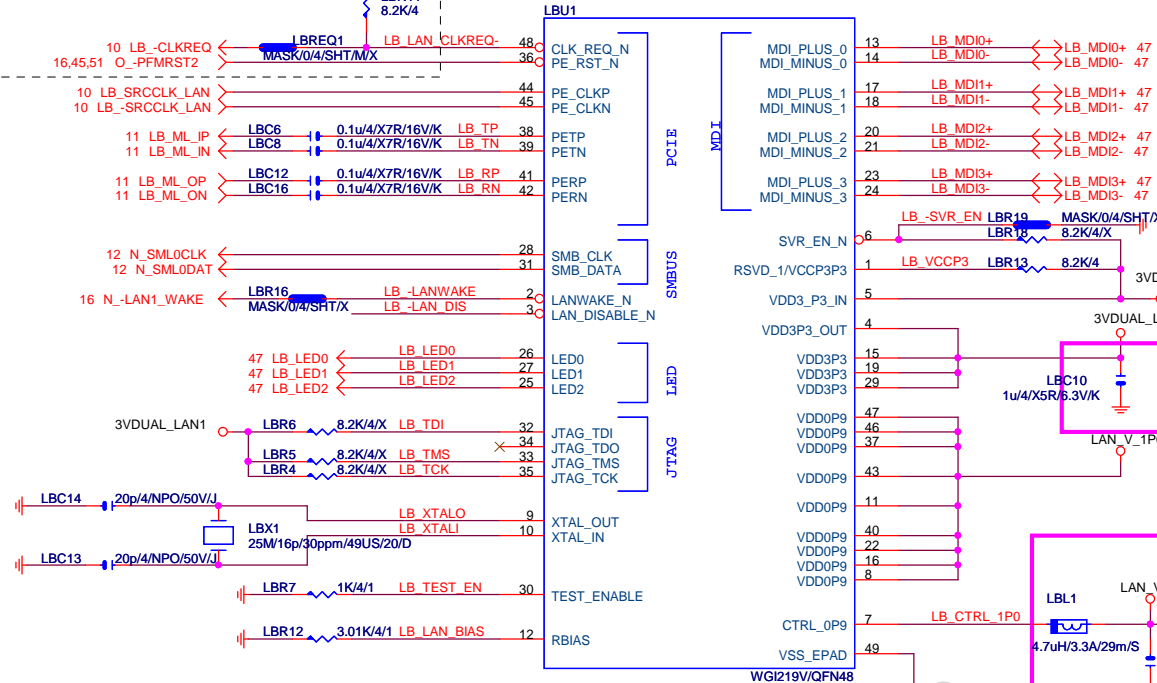
Document Number

**GA-Z270X-GAMING 7**Rev  
1.0

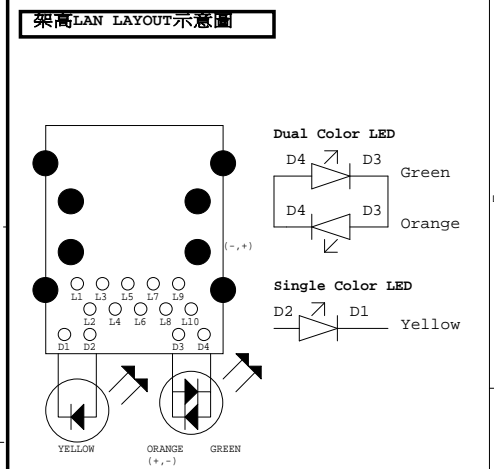
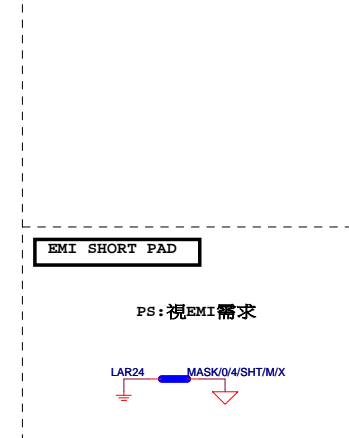
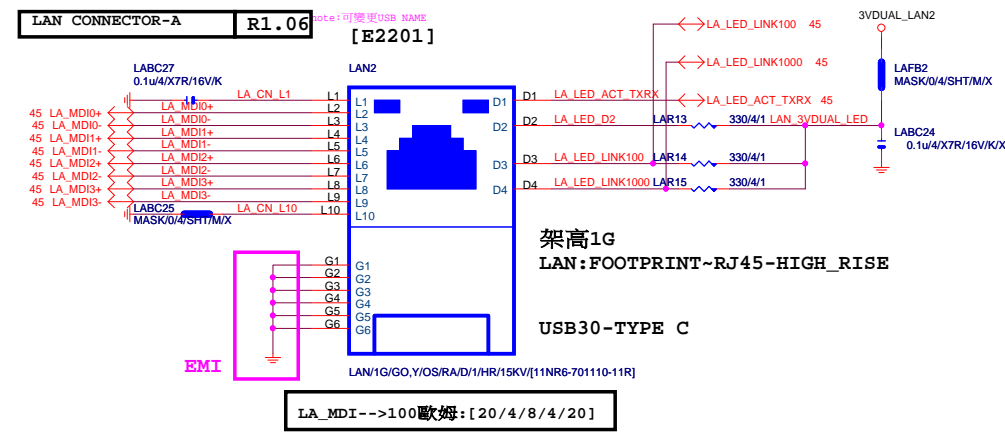
Date: Tuesday, November 22, 2016

Sheet 44 of 76

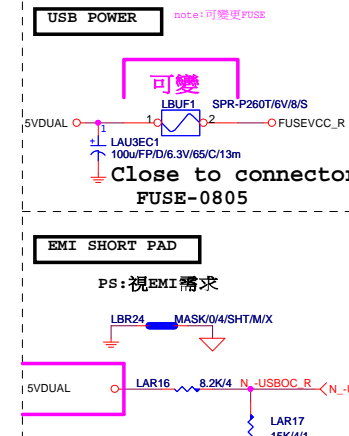
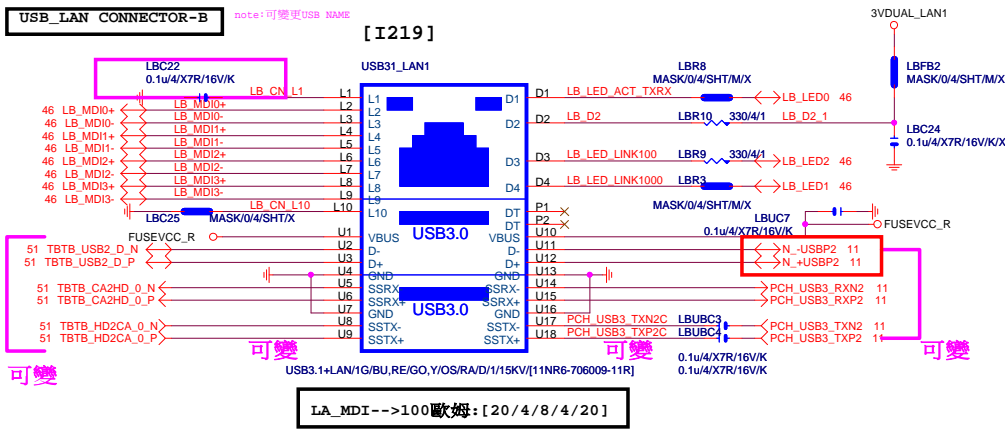






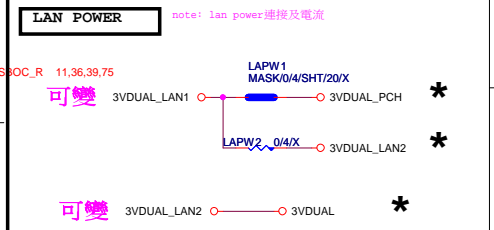
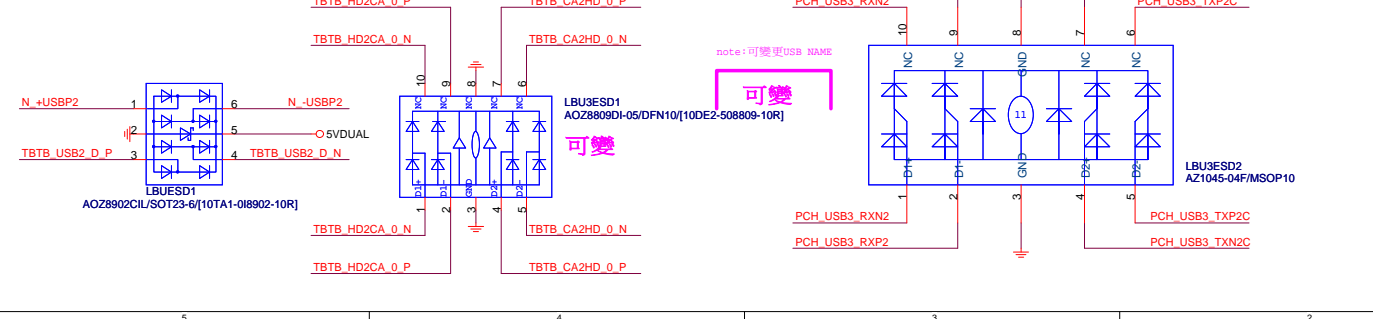


**RMA ESD PROTECT**



- NOTE:**
- 3VDUAL\_LAN1, 3VDUAL\_LAN2 對接POWER供應電流 [目前暫接3VDUAL]
  - USB2.0/3.0 對應USB PORT [目前暫接USB 0,1,2,3 PORT]
  - USB DROOP/DROP E-CAP
  - USB OC線路

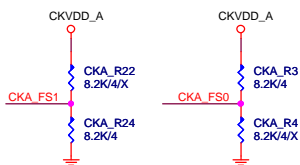
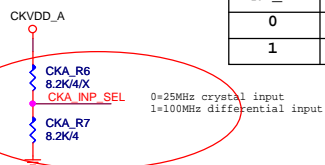
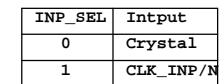
**RMA ESD PROTECT**



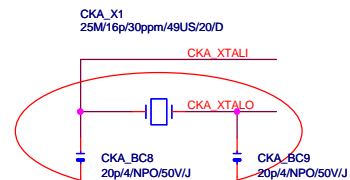
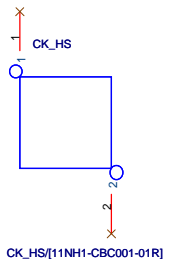
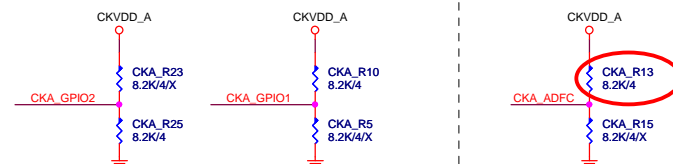
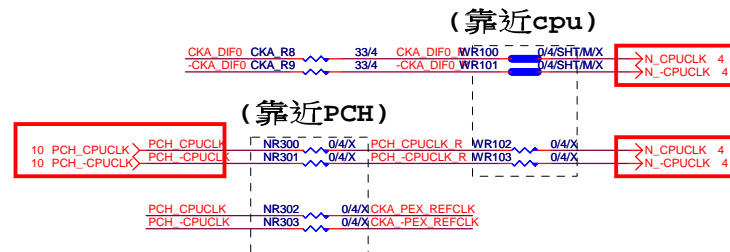
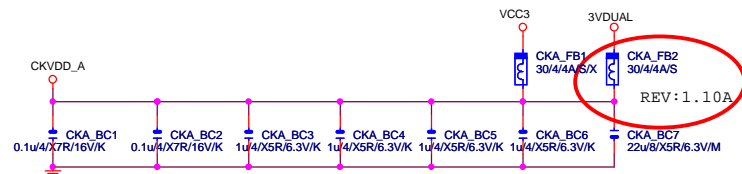
~USB30\_LAN1設定在ERP可LAN WAKEUP

~USB30\_LAN2由獨立LAN POWER L1117供給

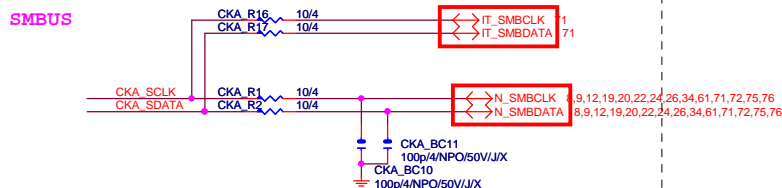
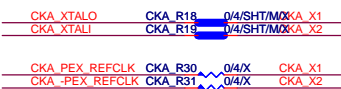
IDT6V41630



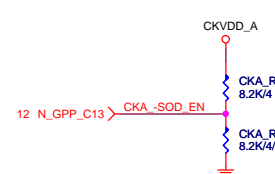
B53b1(FS1)	B53b0(FS0)	VCO (MHz)	CPU Divider	CPU (MHz)	Typ SS%	Typ SS ON/OFF
0	0	200.00	2.00	100.00	-	OFF
0	1	400.00	4.00	100.00	-	OFF
1	0	100.00	10.00	100.00	-0.50%	ON
1	1	100.00	1.00	100.00	-	OFF



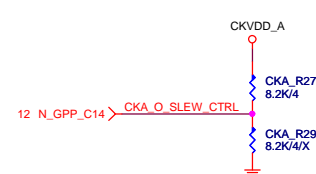
Defaults  
CKX1.CKBC8.CKBC9.CKR18.CKR19上件  
CKR30.CKR31不上件



### Real time selection function



### Frequency change slew rate control



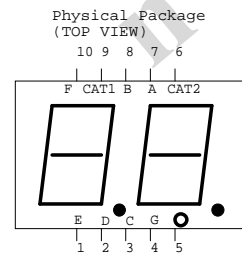
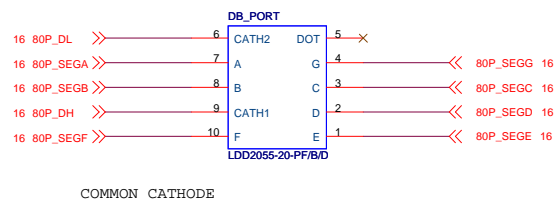
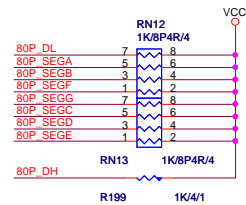
# GIGABYTE™

Title	IDT6V41530_CLK BUFFER
-------	-----------------------

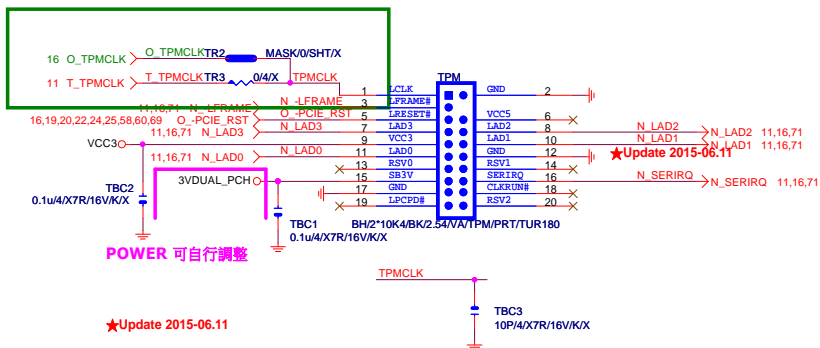
Size	Document Number	Rev
Custom	<b>GA-Z270X-GAMING 7</b>	<b>1.0</b>
Date:	Tuesday, November 22, 2016	Sheet 48 of 76

Rev  
1.0

80 PORT

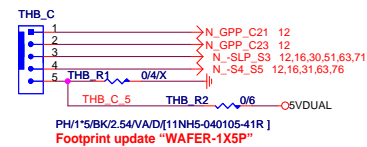


## TPM CONNECT

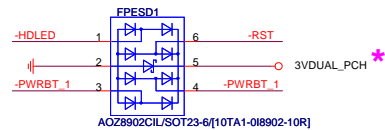


## Thunderbolt

★Update 2015-12-29

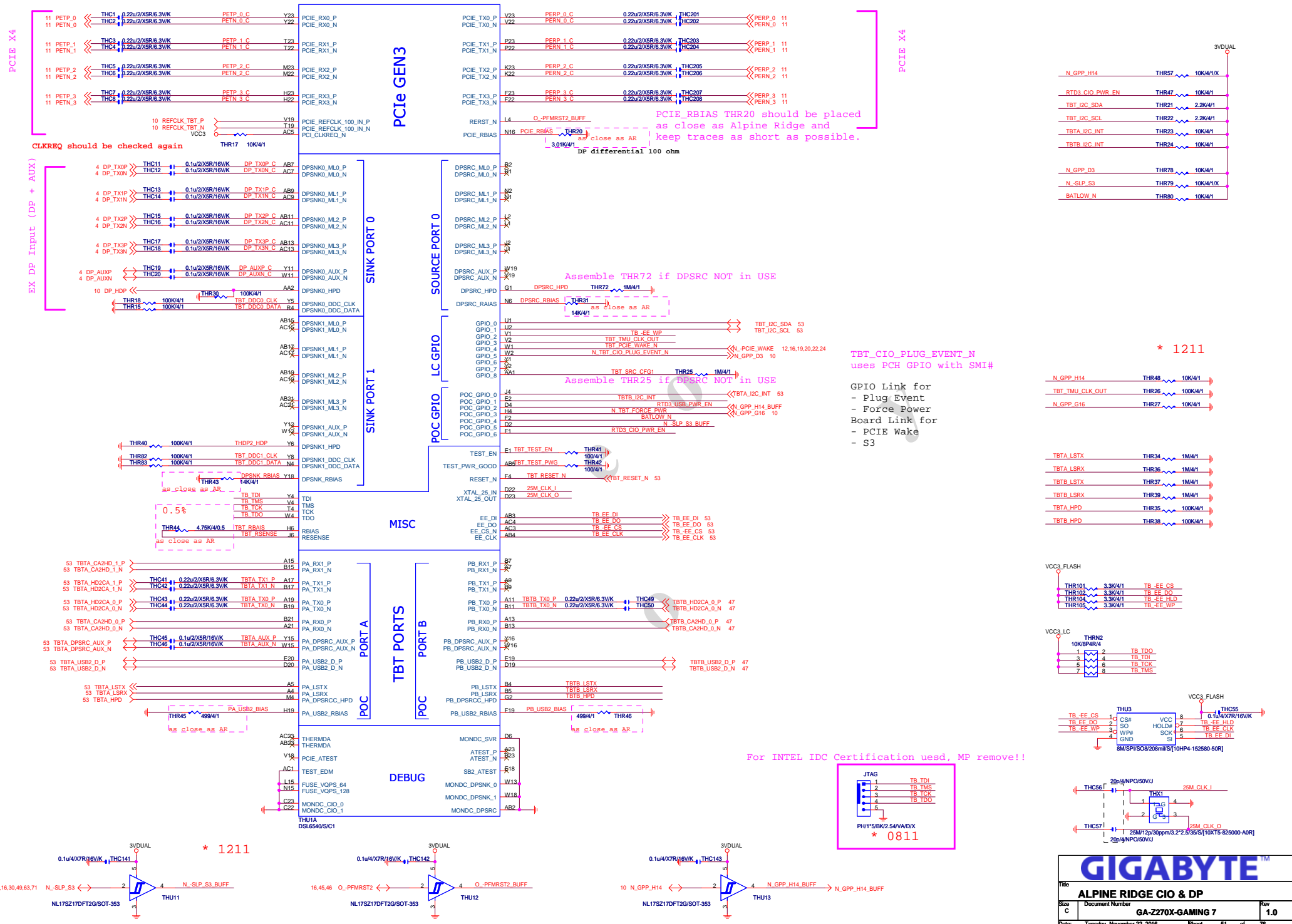
PH/1\*5/BK/2.54/VA/D[11NH5-040105-41R]  
Footprint update: "WAFFER\_4X5R"

### Footprint update "WAFER-1X5P"

[illegible]

INTEL AR module (TBT + U31A) SCH 1.2 (2016/03/28) 4 Layers

Base on INTEL AR reference SCH 1.4 (2015/11/25)

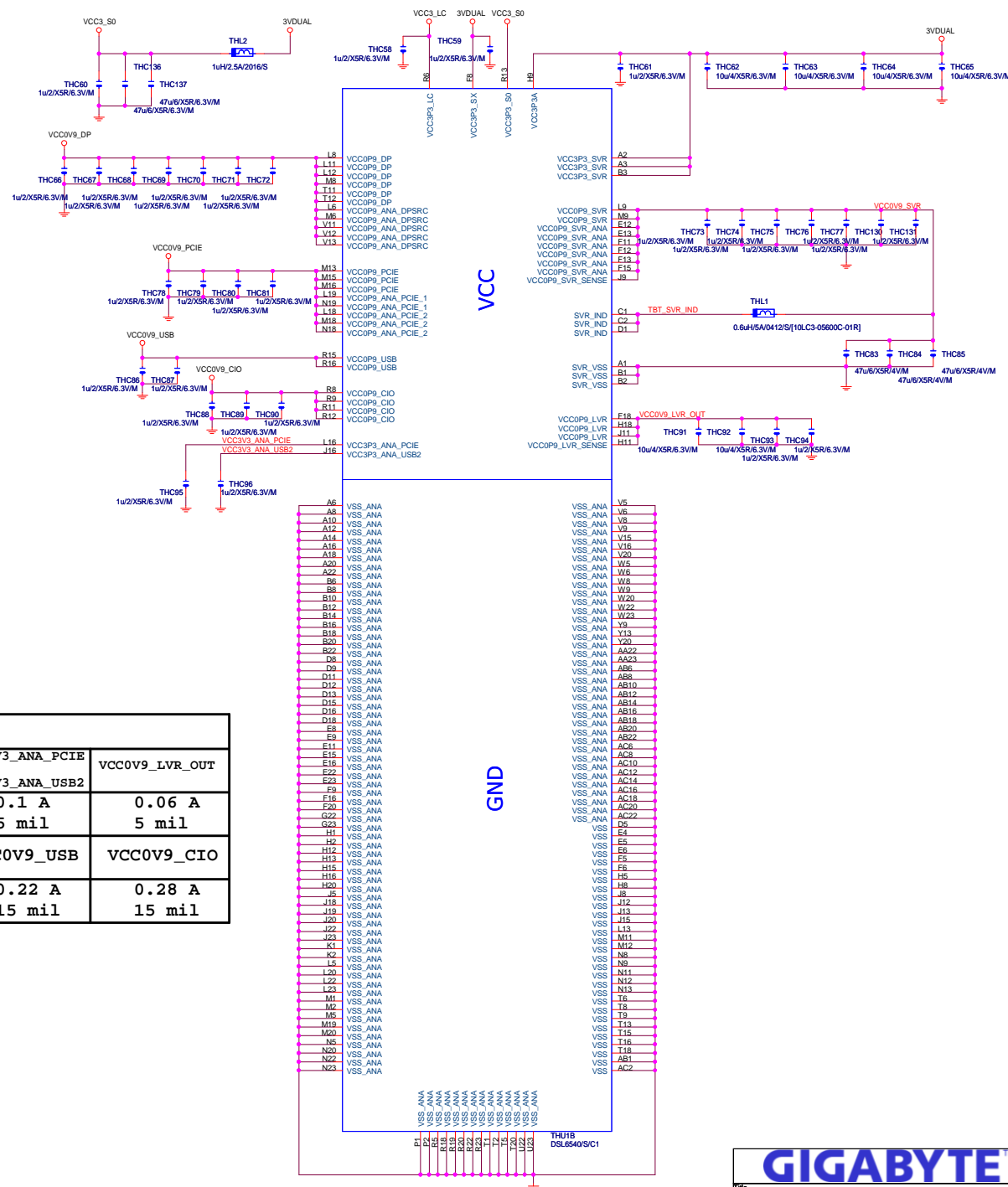


ALPINE RIDGE CIO & DP

Size C Document Number **GA-Z270X-GAMING 7** Rev **1.0**

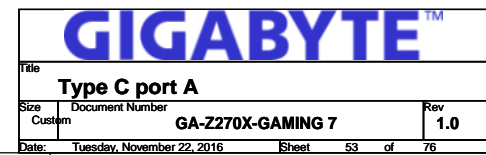
Date: Tuesday, November 22, 2016 Sheet 51 of 76

Base on INTEL AR reference SCH 1.4 (2015/11/25)

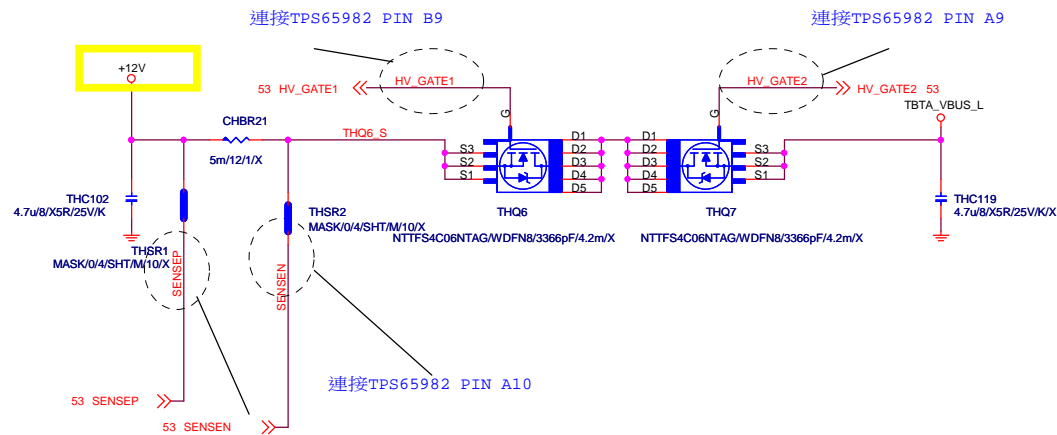


Power Consumption Table					
	VCC3	3VDUAL	VCC3_LC	VCC3V3_ANA_PCIE VCC3V3_ANA_USB2	VCC0V9_LVR_OUT
Max Current(A)	1.05 A 40 mil	0.19 A 10 mil	0.03 A 5 mil	0.1 A 5 mil	0.06 A 5 mil
	VCC0V9_SVR	VCC0V9_DP	VCC0V9_PCIE	VCC0V9_USB	VCC0V9_CIO
Max Current(A)	1.83 A 80 mil	0.7 A 30 mil	0.58 A 30 mil	0.22 A 15 mil	0.28 A 15 mil


Base on INTEL AR reference SCH 1.7 (2016/05/24)





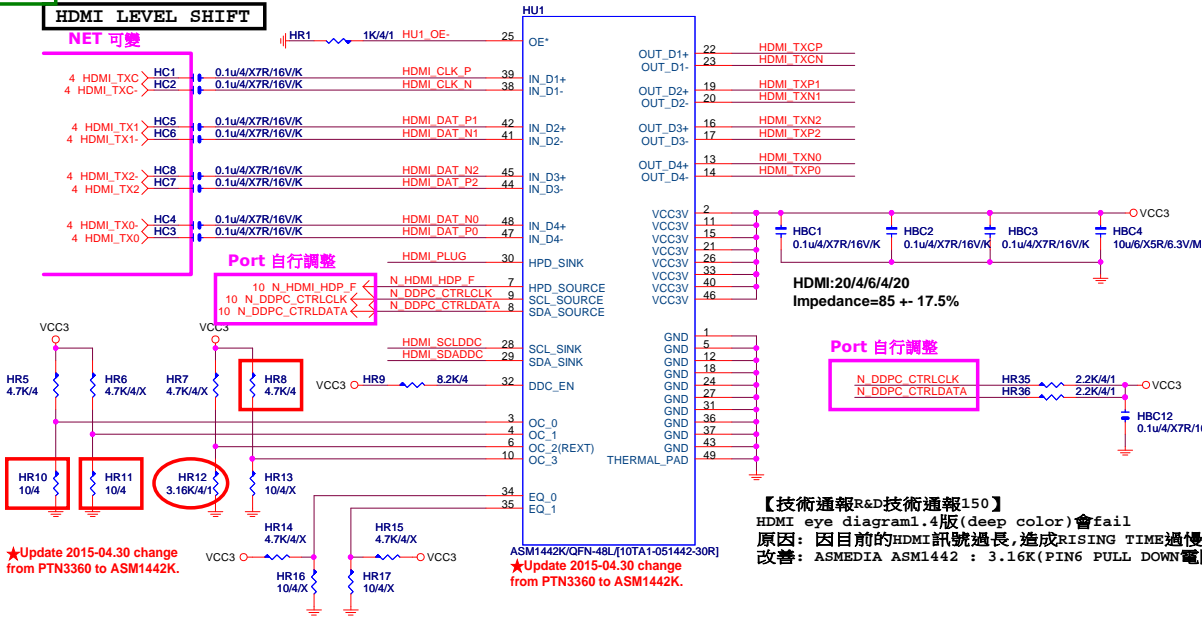


5	4	3	2	1
D				
C				
B				
A				



Title		
DISPLAY PORT IN		
Size	Document Number	Rev
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HDMI LEVEL SHIFT

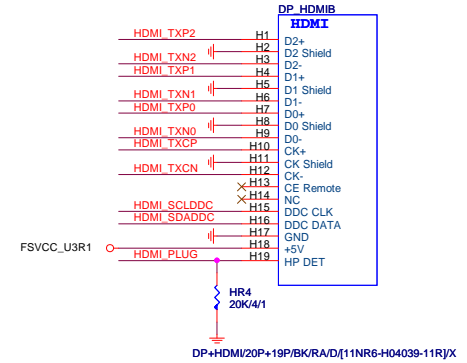
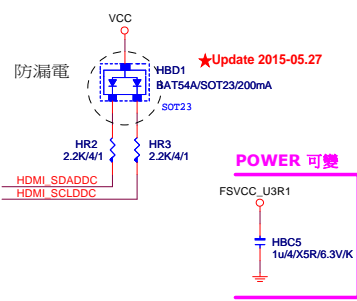


★Update 2015-04.30 change from PTN3360 to ASM1442K.

★Update 2015-04.30 change from PTN3360 to ASM1442K.

PTN3360:PIN 4/10/34/35 NC PIN,都不上值;只上HR12:10K  
ASM1442:紅色框要上,HR12:3.16K

【技術通報R&D技術通報150】  
HDMI eye diagram1.4版(deep color)會fail  
原因: 因目前的HDMI訊號過長,造成RISING TIME過慢,而會壓到eye diagram  
改善: ASMEDIA ASM1442 : 3.16K(PIN6 PULL DOWN電阻) 10ohm(PIN4 PULL DOWN電阻)



GIGABYTE



Rev 0.1

M.2 Lane4 from PCH port26

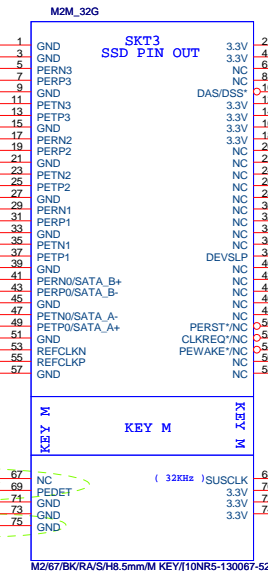
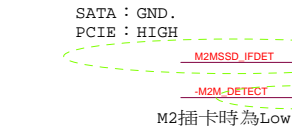
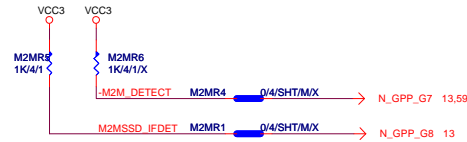
M.2 Lane3 from PCH port25

M.2 Lane2 from PCH port24

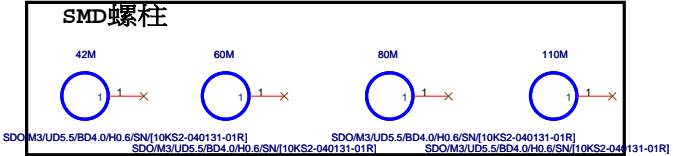
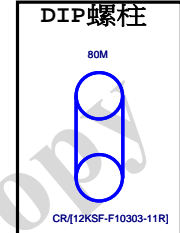
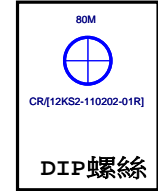
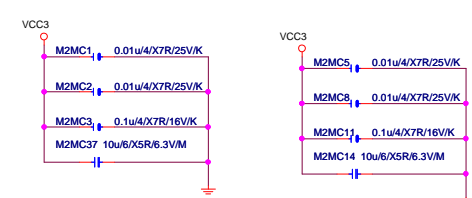
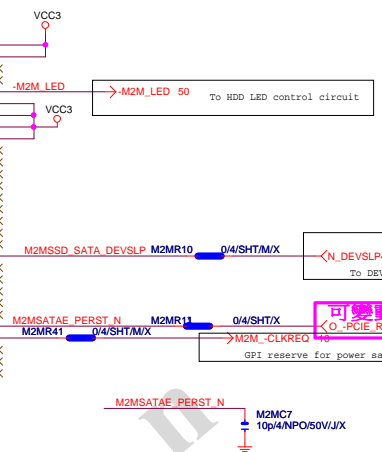
M.2 Lane2 from PCH port23

需與M2\_-CLKREQ對應

支援SATA and M.2 function

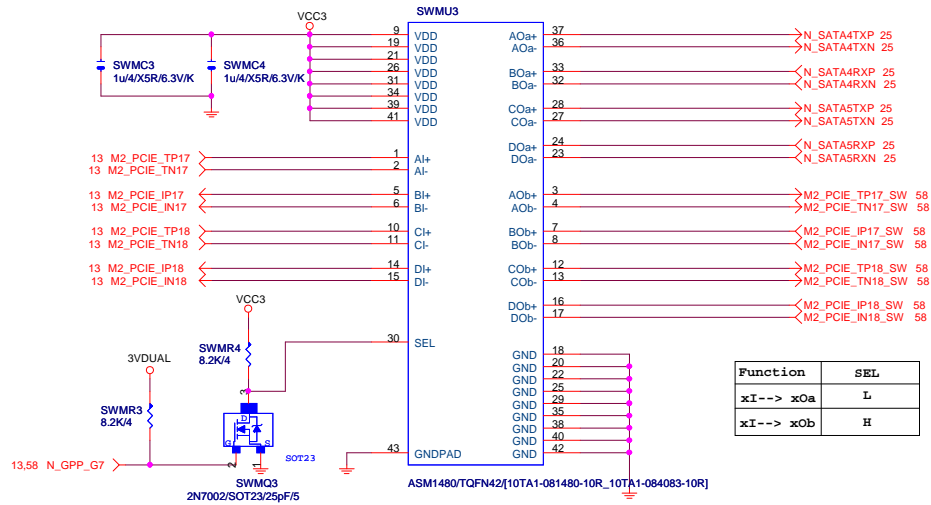


架高



Rev 0.1

(M)TYPE



M.2 Detect N_GPP_G7	M.2 MODE N_GPP_G8	PCIE17	PCIE18	PCIE19	PCIE20
HIGH	X	切回 SATA4	切回 SATA5	N\A	N\A
LOW	HIGH(PCIE)	PCIEX4 FOR M.2(最優先)			
LOW	LOW(SATA)	SATA FOR M.2	N\A	N\A	N\A

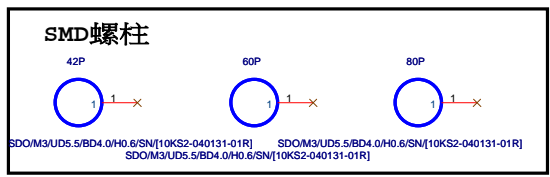
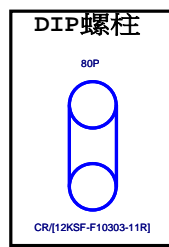
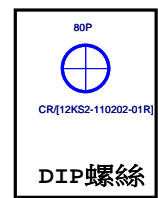
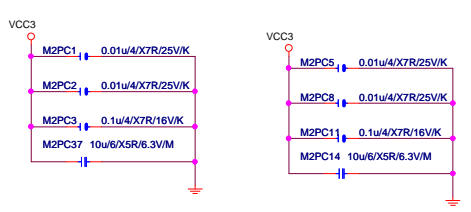
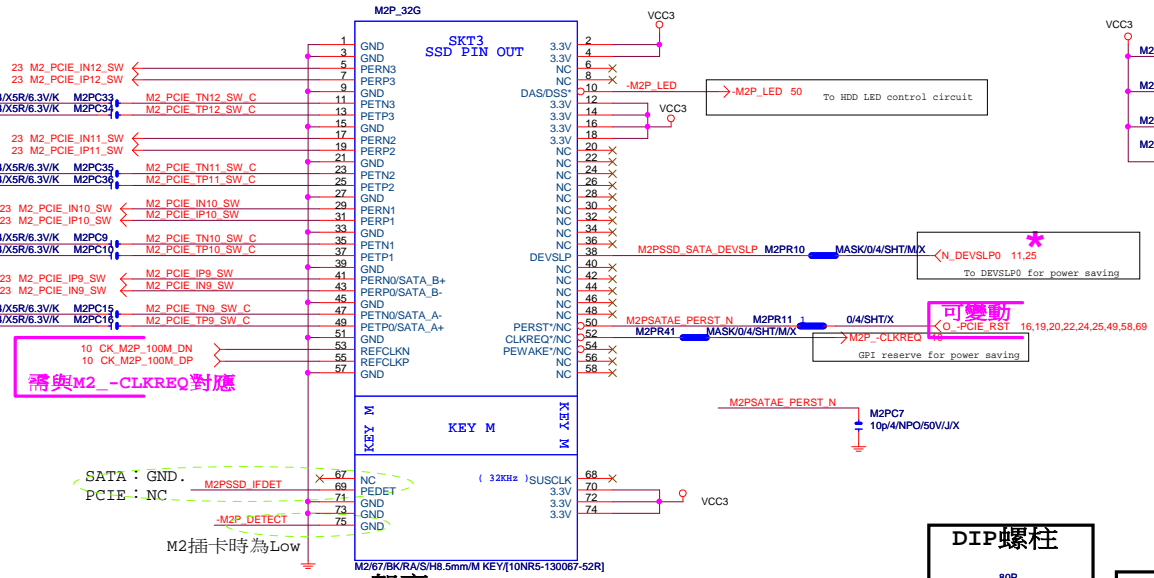
M.2 Lane4 from PCH port12

M.2 Lane3 from PCH port11

M.2 Lane2 from PCH port10

M.2 Lane2 from PCH port9


支援SATA and M.2 function





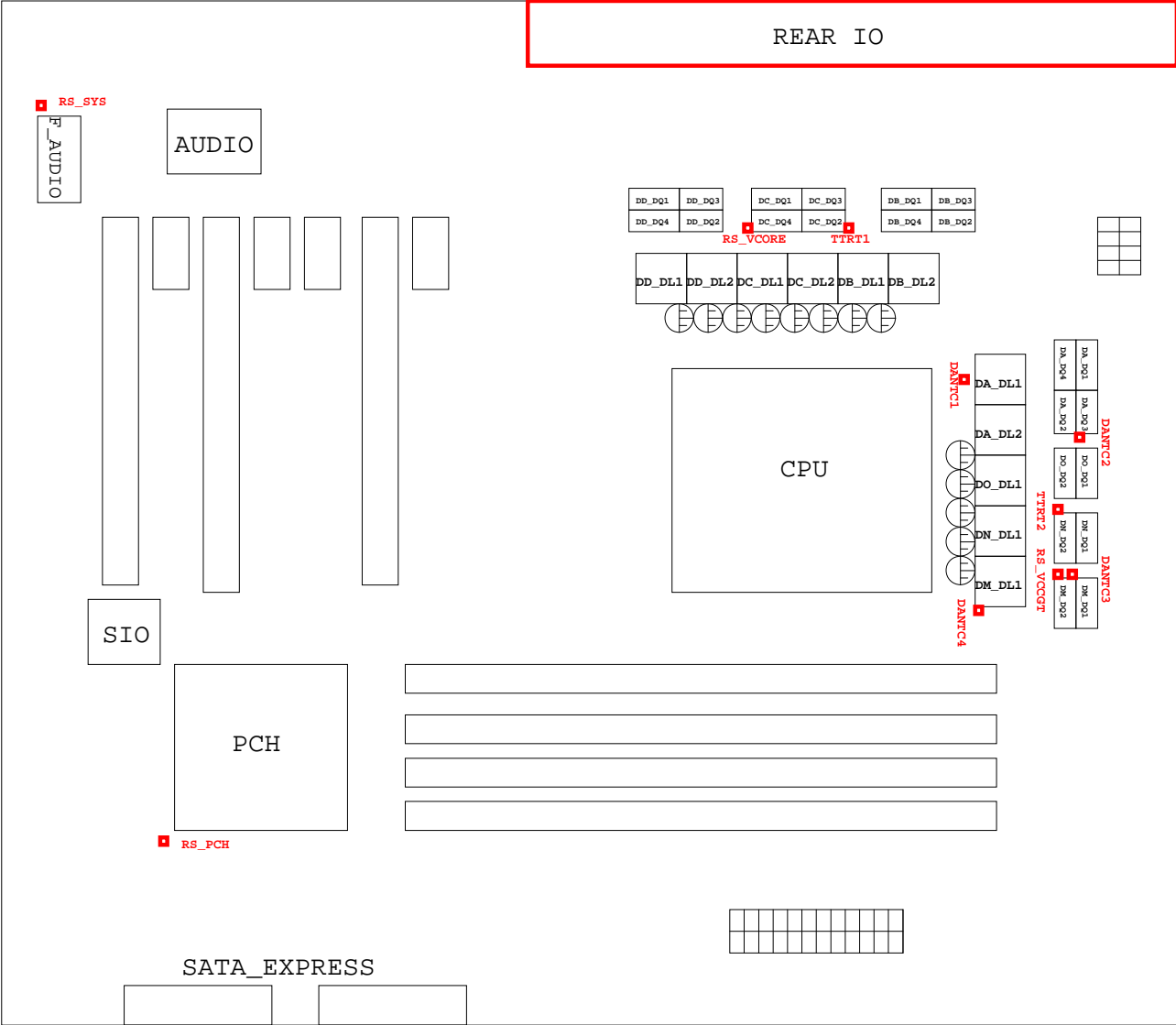


5	4	3	2	1
D				
C				
B				
A				



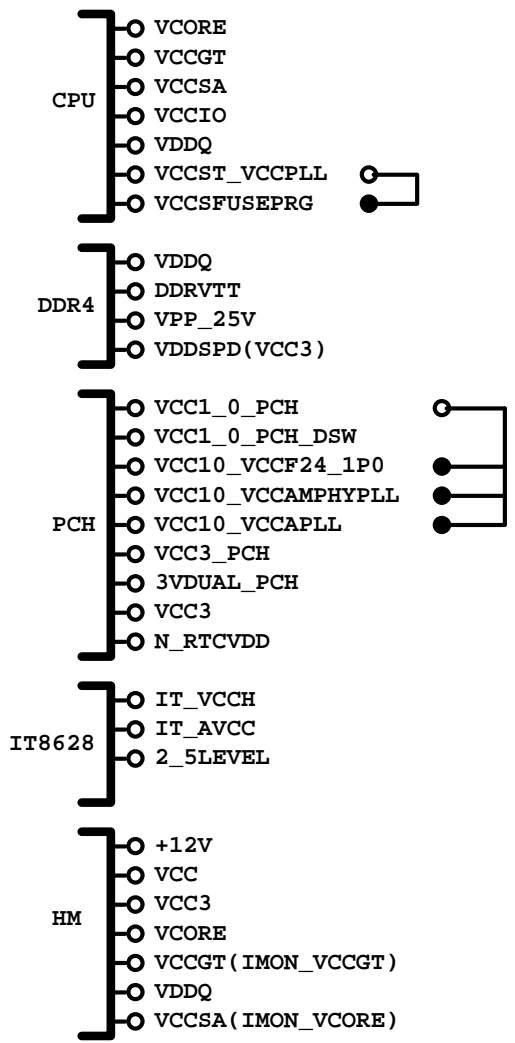
Title		
Renesas uPD720210_1		
Size	Document Number	Rev
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5	4	3	2	1
EMI/ESD		R0.1		
D				D
<div> <div>CLOSE SIO</div> <div> <div>EMIC1</div> <div>100p/4/NPO/50V/J/X</div> <div>12,16,30,49,51,71 N_-SLP_S3</div> </div> <div> <div>EMIC2</div> <div>100p/4/NPO/50V/J/X</div> <div>12,16,31,49,76 N_-S4_S5</div> </div> </div>		<div> <div>CLOSE PCH</div> <div> <div>EMIC3</div> <div>100p/4/NPO/50V/J/X</div> <div>4,12 N_CPUPWROK</div> </div> </div>		
C				C
B				B
A				A
<div> <div>GIGABYTE™</div> <div> <div>Title</div> <div>EMI/ESD</div> </div> <div> <div>Size A</div> <div>Document Number</div> <div>GA-Z270X-GAMING 7</div> </div> <div> <div>Date:</div> <div>Tuesday, November 22, 2016</div> </div> <div> <div>Sheet</div> <div>63</div> <div>of</div> <div>76</div> </div> <div> <div>Rev</div> <div>1.0</div> </div> </div>				
5	4	3	2	1

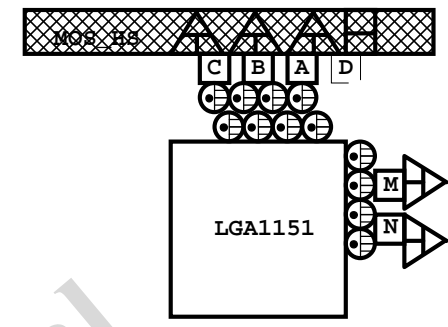
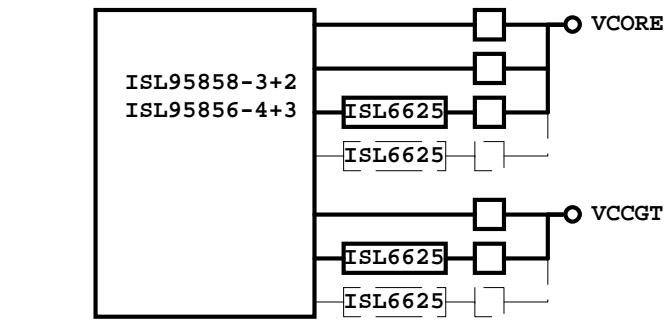


熱敏電阻	擺放靠近位置	走線方式
DANTC1	DA_DL2	Differential
DANTC2	DA_DQ3	Differential
DANTC3	DM_DQ2	Differential
DANTC4	DM_DL1	Differential
RS_VCORE	DC_DQ4	N/A
RS_VCCGT	DM_DQ2	N/A
TTRT1	DC_DQ2	N/A
TTRT2	DM_DQ2	N/A
RS_PCH	PCH	N/A
RS_SYS	F_AUDIO	N/A

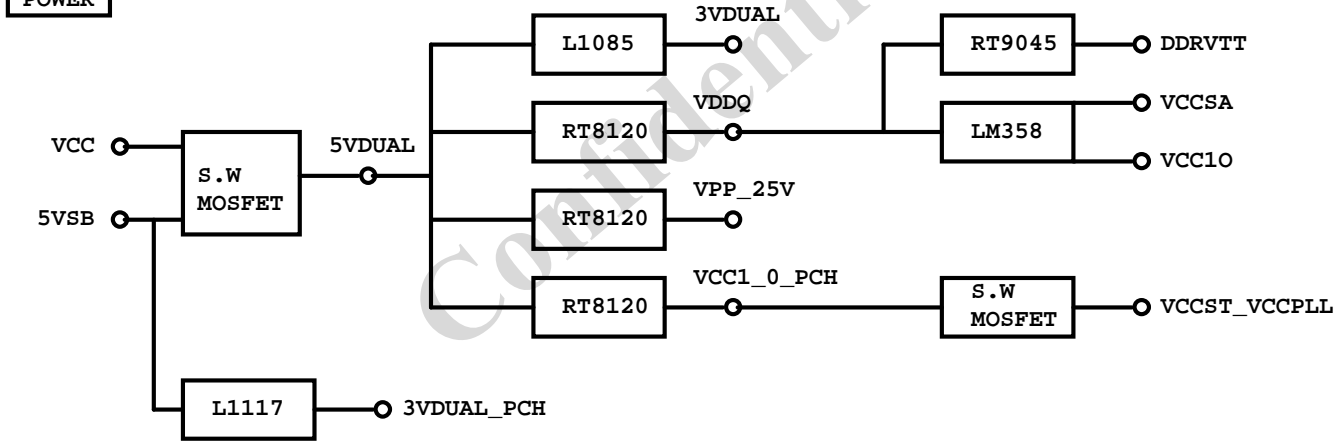
# POWER BLOCK MAP



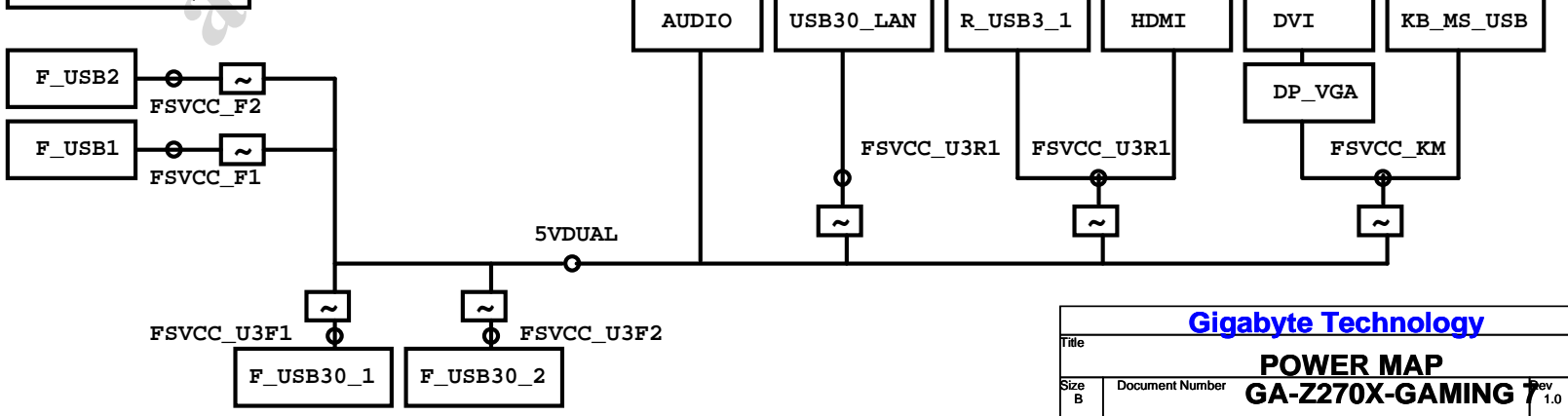
# VCORE/VCCGT



# POWER



# FUSE POWER F/R



固態電容料號.請自行修改

日系黑色固態	Capture Value
11C02-C85600-01R	560u/FP/D/6.3V/68/C/8m
11C05-C82700-01R	270u/FP/D/16V/88/C/12m
11C05-C61000-01R	100u/OS/D/16V/66/C/30m
11C02-C51000-01R	100u/FP/D/6.3V/65/C/13m

日系一般固態	Capture Value
11C02-685600-01R	560u/FP/D/6.3V/68/8m
11C05-882700-01R	270u/FP/D/16V/88/12m
11C05-661000-03R	100u/OS/D/16V/66/30m
11C02-651000-02R	100u/OS/D/6.3V/66/30m

台系固態	Capture Value
11C02-661000-09R	100u/OS/D/6.3V/66/A/35m
11C05-691000-09R	100u/OS/D/16V/69/A/35m
11C05-8C2700-09R	270u/FP/D/16V/8C/A/10m
11C02-695600-09R	560u/FP/D/6.3V/69/A/11m

PWM料號

		料號	Capture Value	Footprint
PWM	ISL95856	10TA1-695856-01R		IC52QFN-6x6-G
PWM	ISL95858	10TA1-695858-01R		IC52QFN-6x6-G
PWM	IR35201	10TA1-635201-00R		IC56QFN-9VRS4339
PWM	IR3570	10TA1-603570-00R		IC40MLFP-ISL95835
PWM	RT8237C/D	10TA1-608237-01R		IC10DFN-NIS5132

REGULATOR

		料號	Capture Value	Footprint
	NCT3103S	10GL2-203103-01R	NCT3103S/SOP8/2A	IC8-EP5OIC

IRON CHOKE

	料號	Capture Value	SIZE	Footprint	
DIP	11LC5-M4500C-01R	0.5uH/40A/IMD109/M/D	10*10	CH0KE05U-40A-1PQ-3	閃電P
DIP	11LC5-M4500C-11R	0.5uH/40A/IMD109/M/NP/D	10*10	CH0KE05U-40A-1PQ-3	無閃電P
DIP	11LC5-M2500C-01R	0.5uH/20A/IMD0809/M/D	8*8	CH0KE1U-R50M-IF	

Skylake Iron Choke閃電P導入機種如下:  
[1] Z170/H170 機種全部導入  
[2] B150/H110Gaming機種導入, 其餘不導入

Ferrite

	料號	Capture Value	SIZE	Footprint
DIP	11LC5-F3500C-11R	0.5uH/32A/ INCG109/FSI/D	10*10	CH0KE05U-40A-1PQ-3
DIP	11LC5-F2500C-11R	0.5uH/25A/ INC0809/F/D	8*8	CH0KE1U-R50M-IF
SMD	10LC5-F4300C-01R	0.3uH/40A/SIUC/FR/S	10*7	CH0KE11X8MM-SMD

BEAD

	料號	Capture Value	SIZE	Footprint
DIP	10LFB-15470A-01R	47/4030/15A/S	4*3	BEADC8B-BPH_SMD

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Title

RT8120\_DDR4 POWER

Size

Custom

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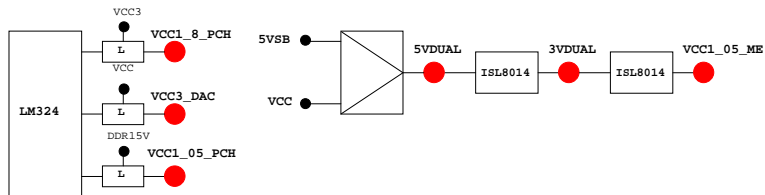
Rev

1.0

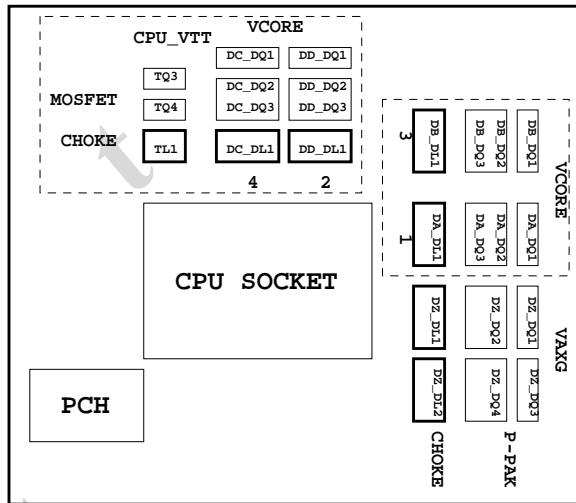
## Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRX1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSS11	SB_LED1_C	
PD4/GP74/BUSS12	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSS10	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VIDO5/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VBSBW#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AFD#/GP86/SMB_C_R	2X PIN	FST_2X8
INIT#/GP85/SMB_D	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VID01/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMB_C_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRX2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下：



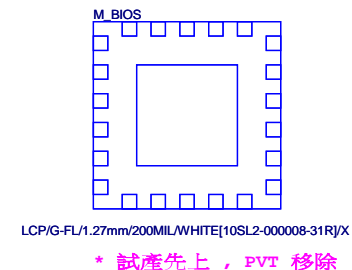
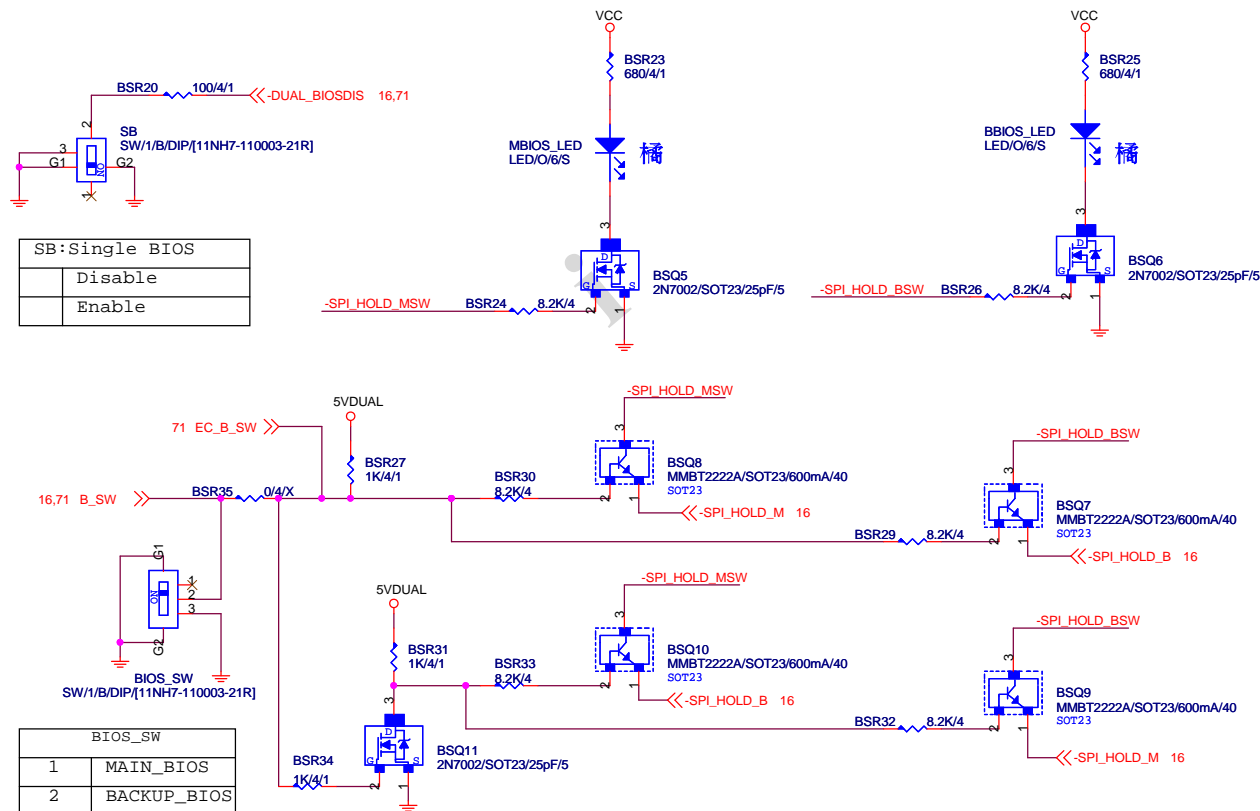
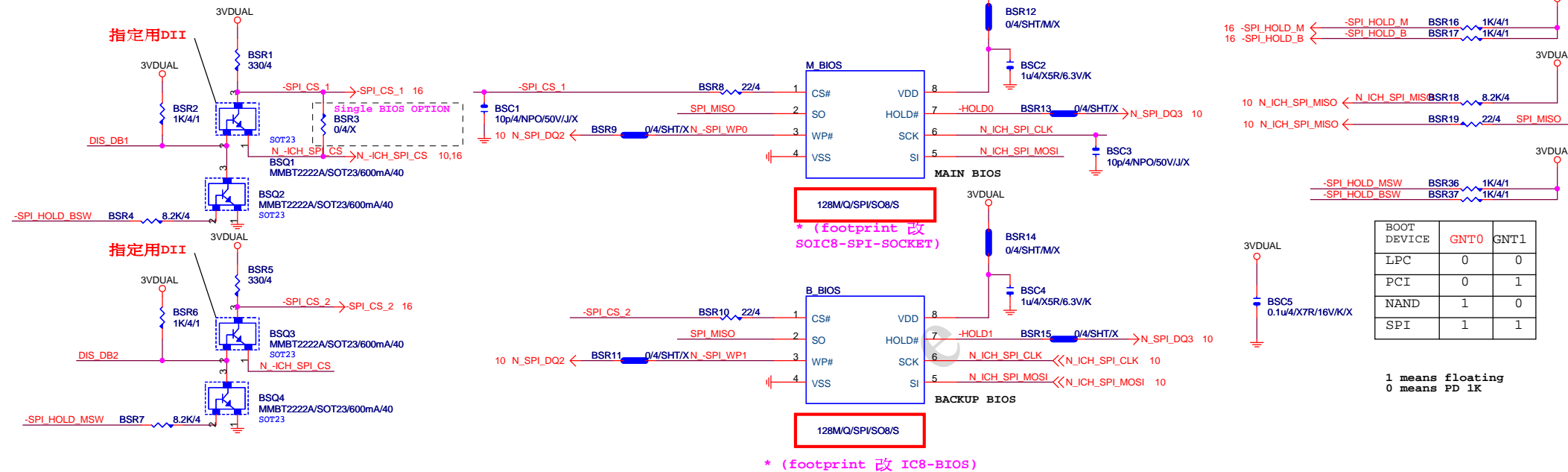
### BIOS超電壓對應表:

散熱模組料號:

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Termination
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

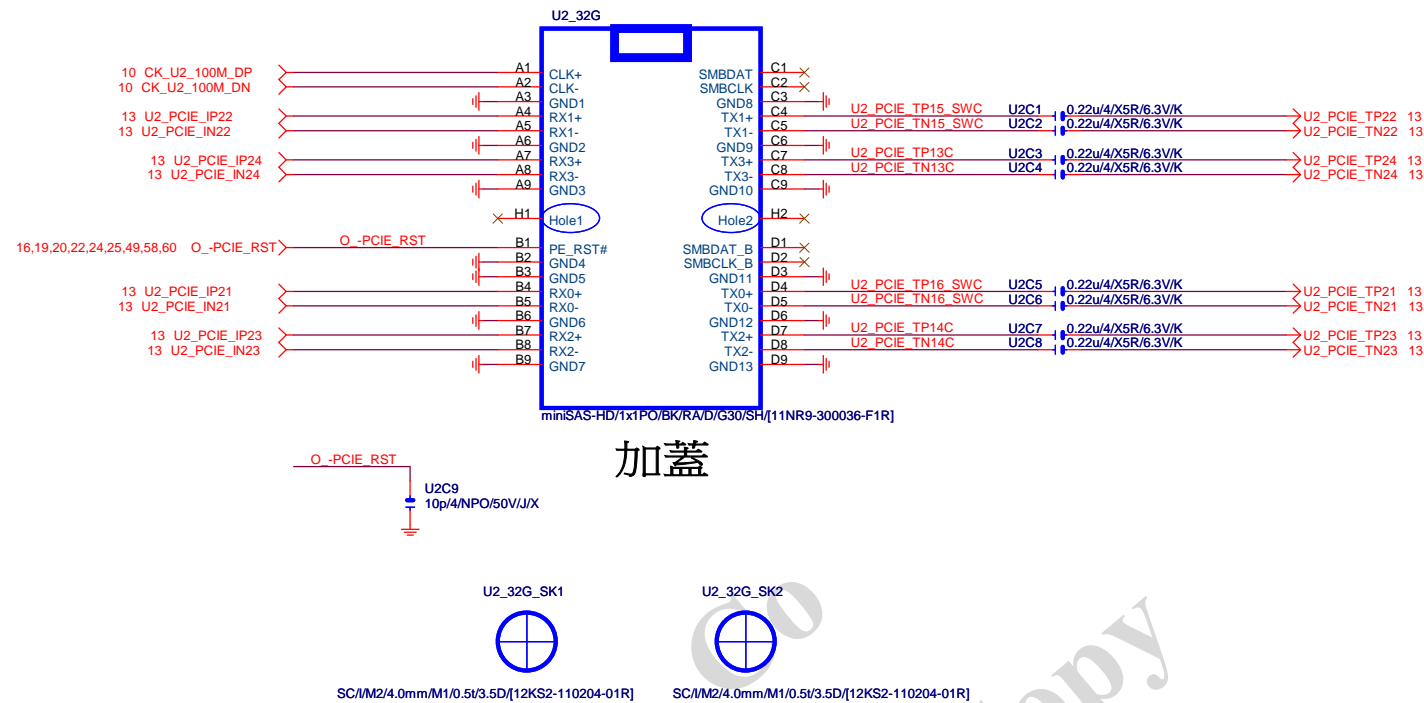
	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

## DUAL BIOS



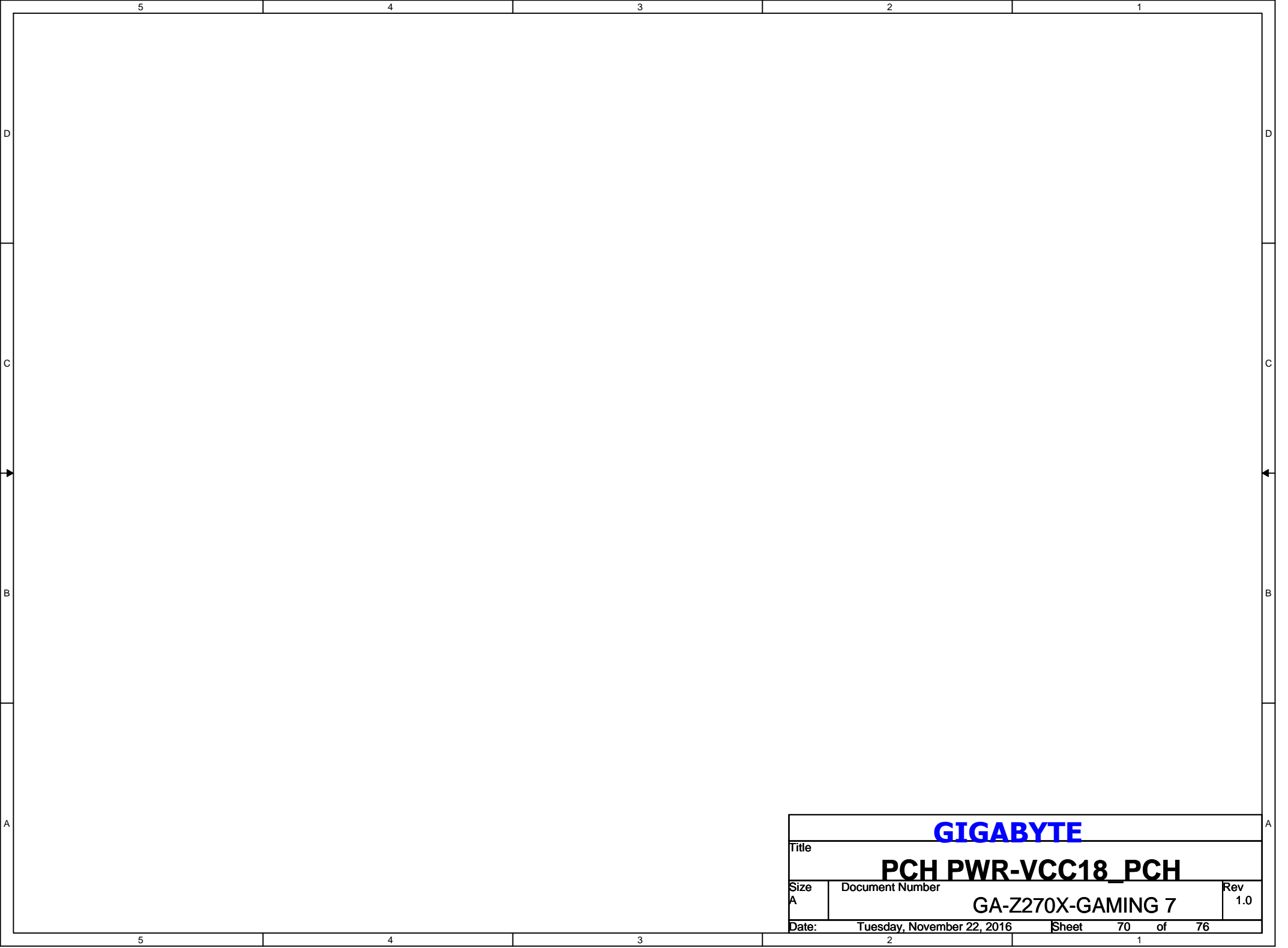


Rev 0.3

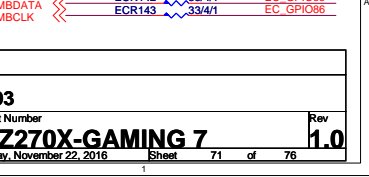
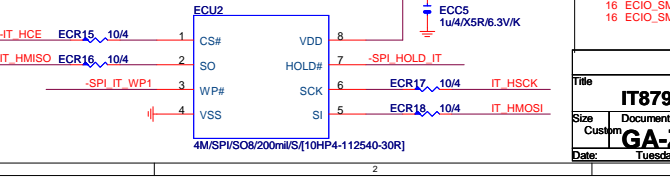
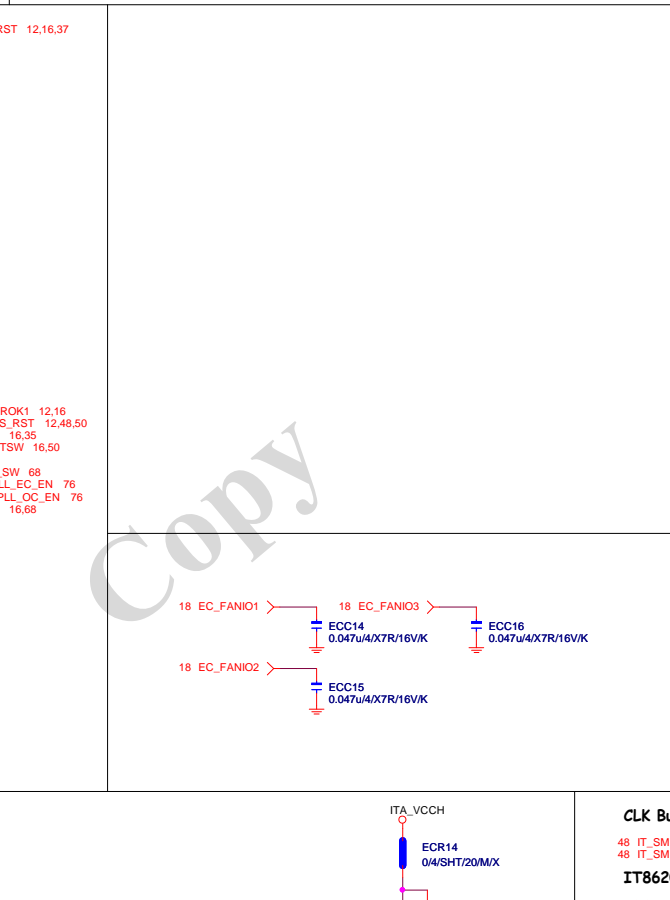
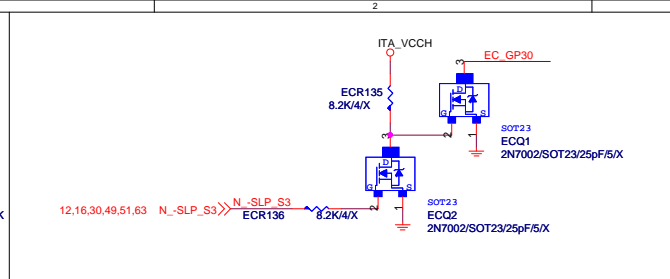


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Title		
M.2 to MINISAS		
Size B	Document Number	Rev
	GA-Z270X-GAMING 7	1.0
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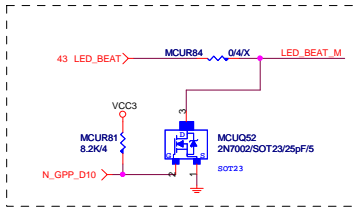
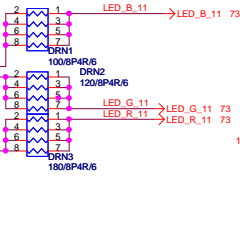
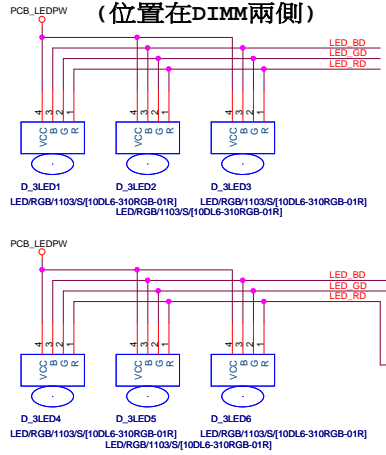


GIGABYTE		
Title		
PCH PWR-VCC18_PCH		
Size	Document Number	Rev
A	GA-Z270X-GAMING 7	1.0
Date:	Tuesday, November 22, 2016	Sheet 70 of 76



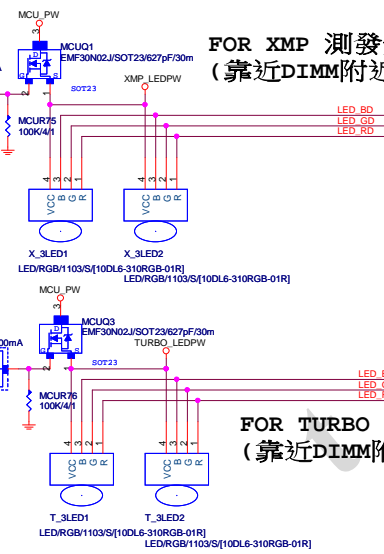
第一區 LED

FOR DIMM 側發光 LED\*6  
(位置在DIMM兩側)

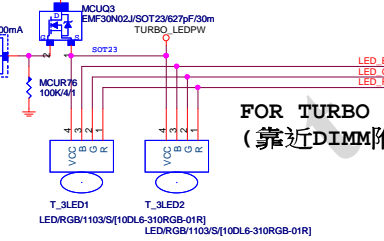


N_GPP_A17	CPU DEBUG
N_GPP_A18	DDR DEBUG
N_GPP_A19	VGA DEBUG
N_GPP_A20	BOOT DEBUG
N_GPP_A21	XMP LED SWITCH
N_GPP_A22	TURBO LED SWITCH
N_GPP_D12	LED_IO LED SWITCH
N_GPP_D15	LED_C LED SWITCH
N_GPP_D17	PCIEX16 LED SWITCH
N_GPP_D18	PCIEX8 LED SWITCH

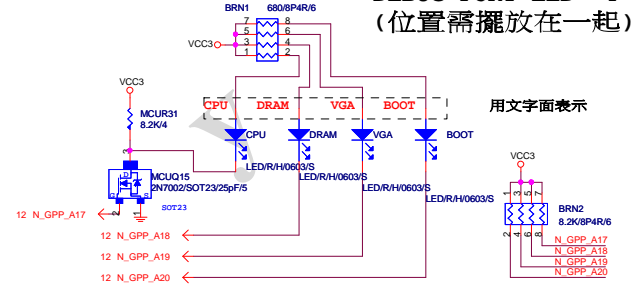
FOR XMP 測發光 LED\*2  
(靠近DIMM附近放背板鑲空)



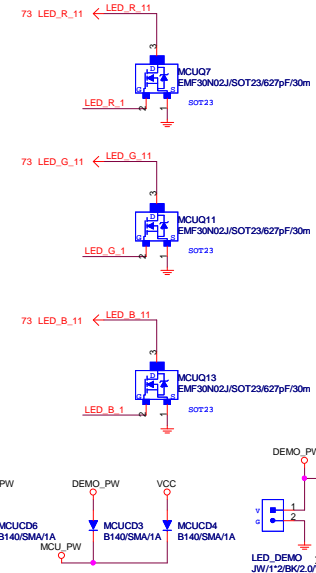
FOR TURBO 測發光 LED\*2  
(靠近DIMM附近背板鑲空)



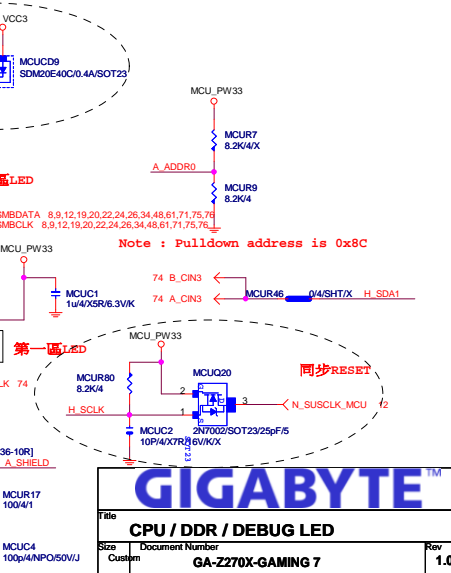
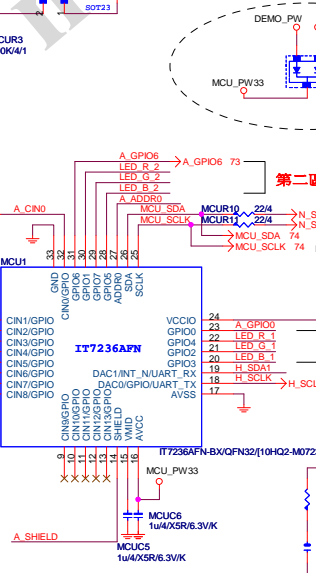
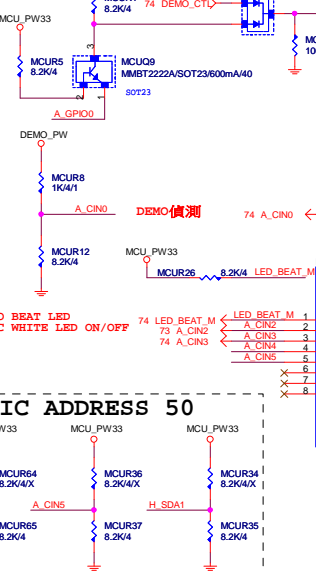
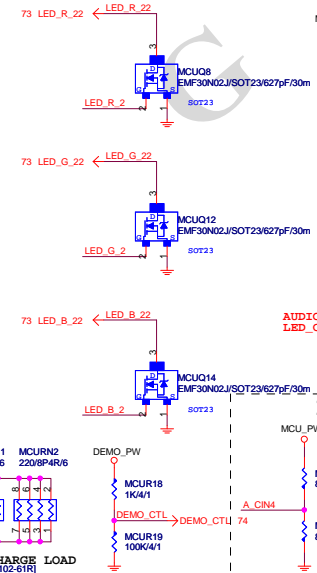
DEBUG PORT LED \*4  
(位置需擺放在一起)



第一區 LED CONTROL



第二區 LED CONTROL



**GIGABYTE**

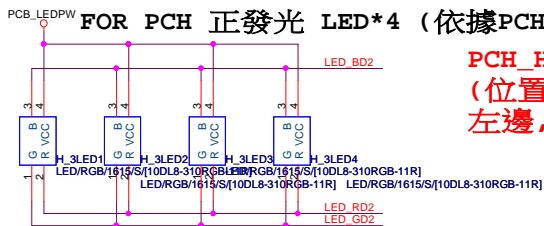
File: CPU / DDR / DEBUG LED  
Size: Custom  
Date: Tuesday, November 22, 2016  
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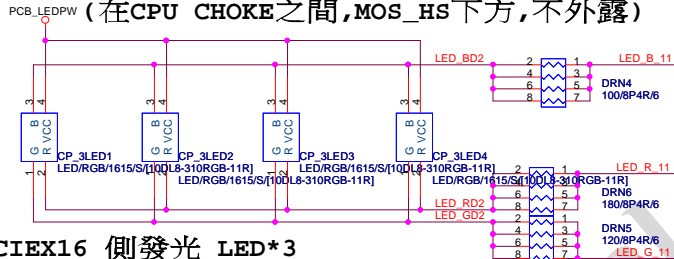
# 第一區 LED

FOR PCH 正發光 LED\*4 (依據PCH\_HS設計擺放)

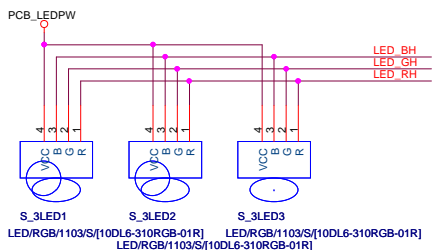
**PCH HS LED**  
(位置靠近PCH\_HS  
左邊,放在PCH\_HS外面)



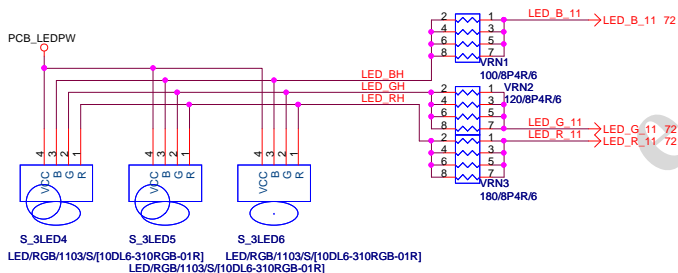
FOR CPU 正發光 LED\*4  
(在CPU CHOKE之間,MOS\_HS下方,不外露)



FOR PCIEX16 側發光 LED\*3  
(位置在PCIEX16 SLOT)

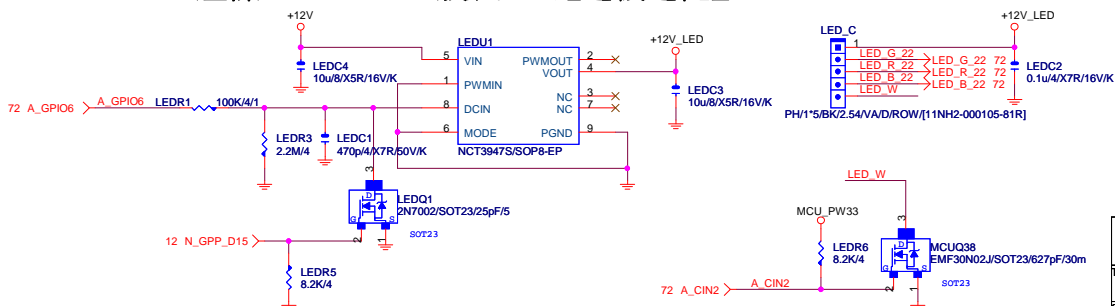


FOR PCIEX8 側發光 LED\*3  
(位置在PCIEX8 SLOT)



# 第二區 LED

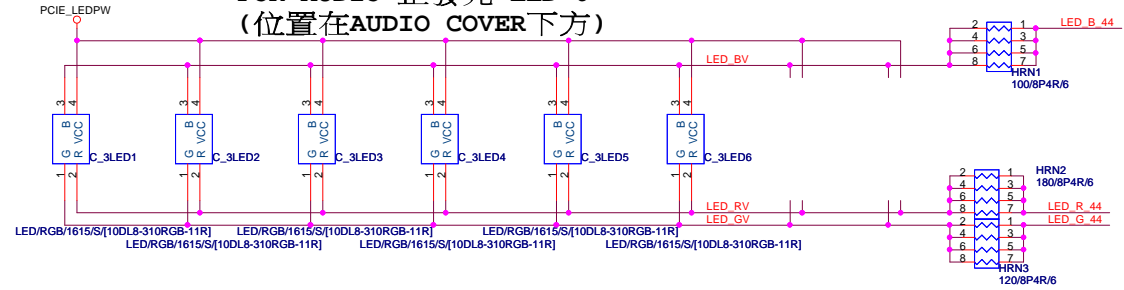
FOR 燈條 LED (LED\_C放在PCB左邊板邊位置)



### 第三區 LED

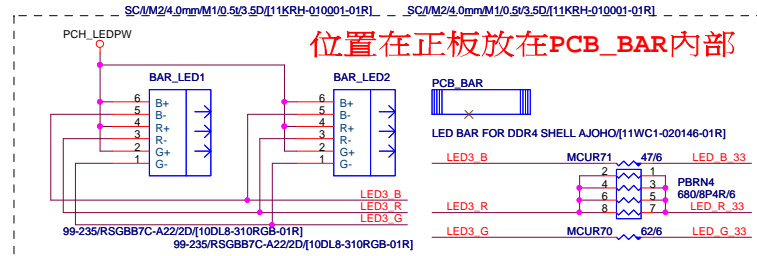
### 第四區 LED

FOR AUDIO 正發光 LED\*6  
(位置在AUDIO COVER下方)



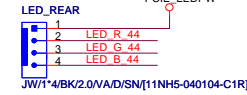
PCB\_BAR\_K1

PCB\_BAR\_K2



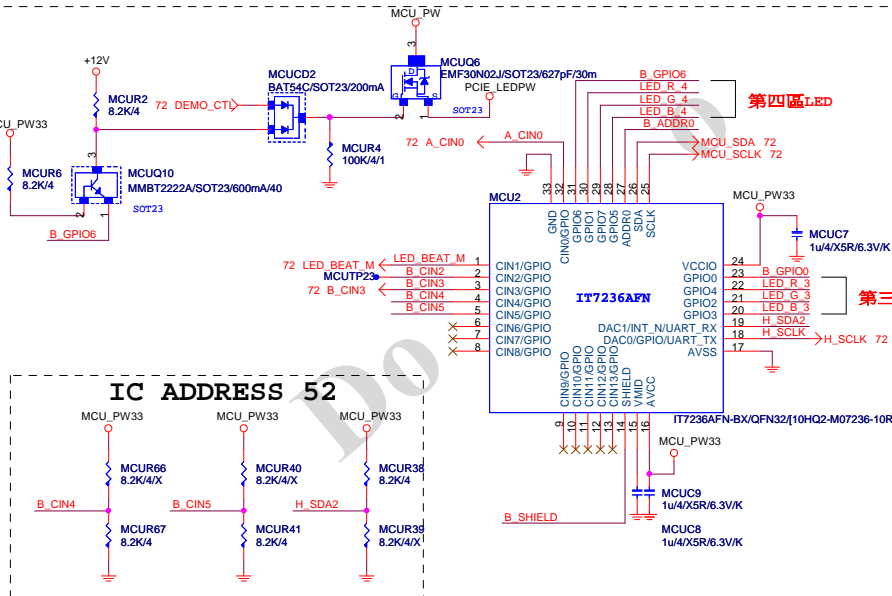
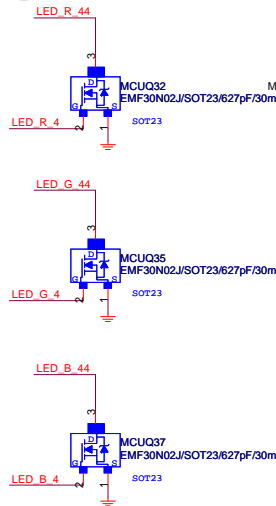
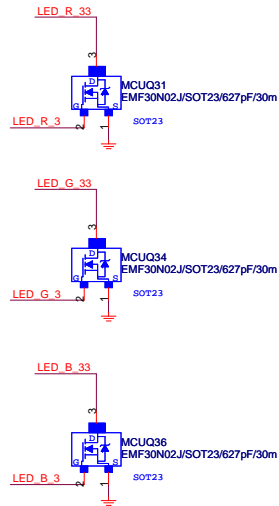
位置在正板放在PCB\_BAR內部

REAR 裝甲LED  
(位置在後窗裝甲內)



### 第三區 LED CONTROL

### 第四區 LED CONTROL



IC ADDRESS 52

第四區LED

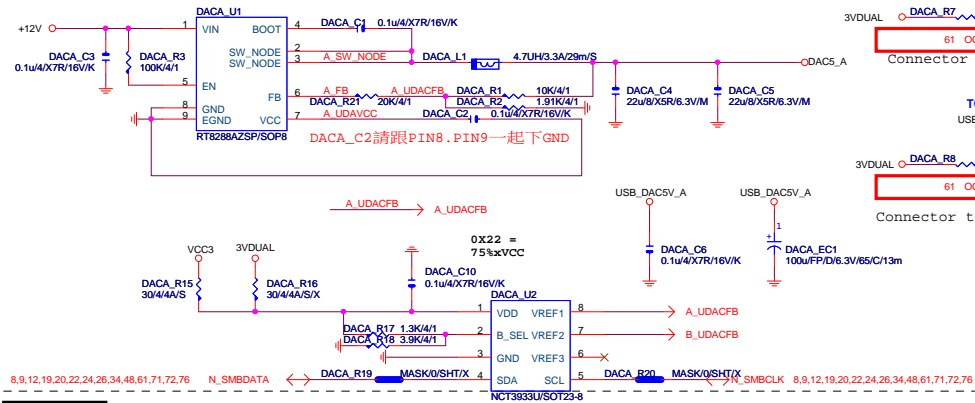
第三區LED

Note : Pullhigh address is 0x8C

# USB\_DAC\_A

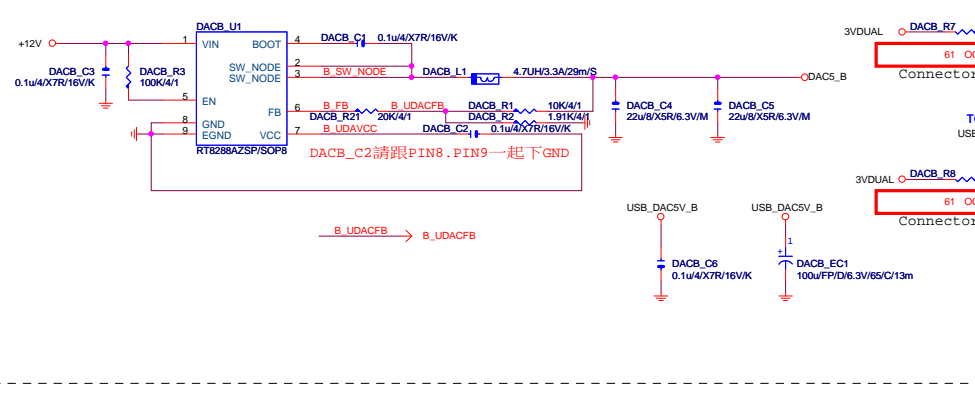
REV:0.1

## F\_USB30\_1



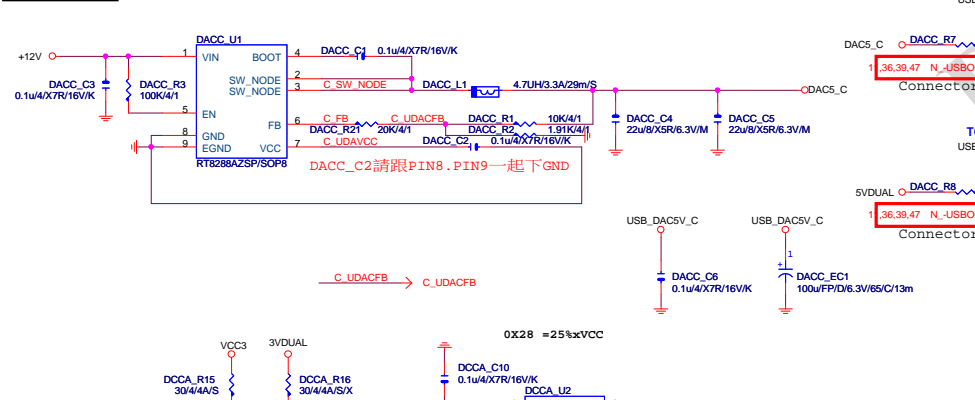
# USB\_DAC\_B

## F\_USB30\_2



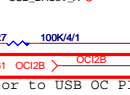
# USB\_DAC\_C

## KB\_MS\_USB30



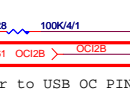
# TO USB\_DAC PORT

USB\_DAC5V\_A



# TO USB\_DAC PORT

USB\_DAC5V\_B



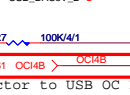
# TO USB\_DAC PORT

USB\_DAC5V\_C



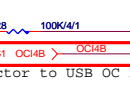
# TO USB\_DAC PORT

USB\_DAC5V\_D



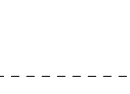
# TO USB\_DAC PORT

USB\_DAC5V\_E



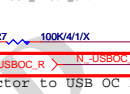
# TO USB\_DAC PORT

USB\_DAC5V\_F



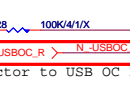
# TO USB\_DAC PORT

USB\_DAC5V\_G



# TO USB\_DAC PORT

USB\_DAC5V\_H



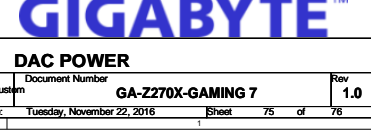
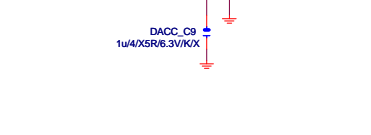
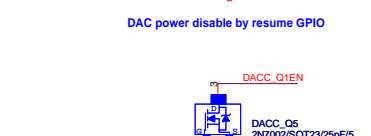
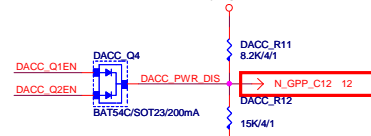
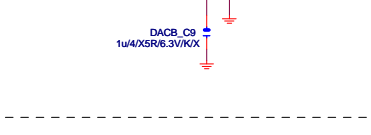
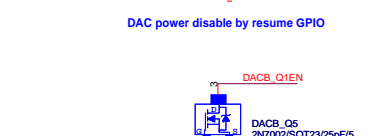
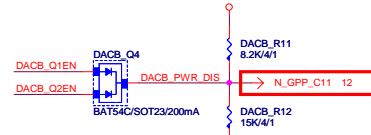
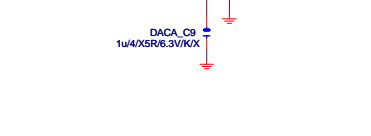
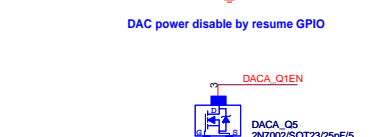
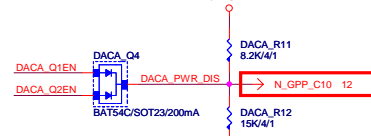
# TO USB\_DAC PORT

USB\_DAC5V\_I

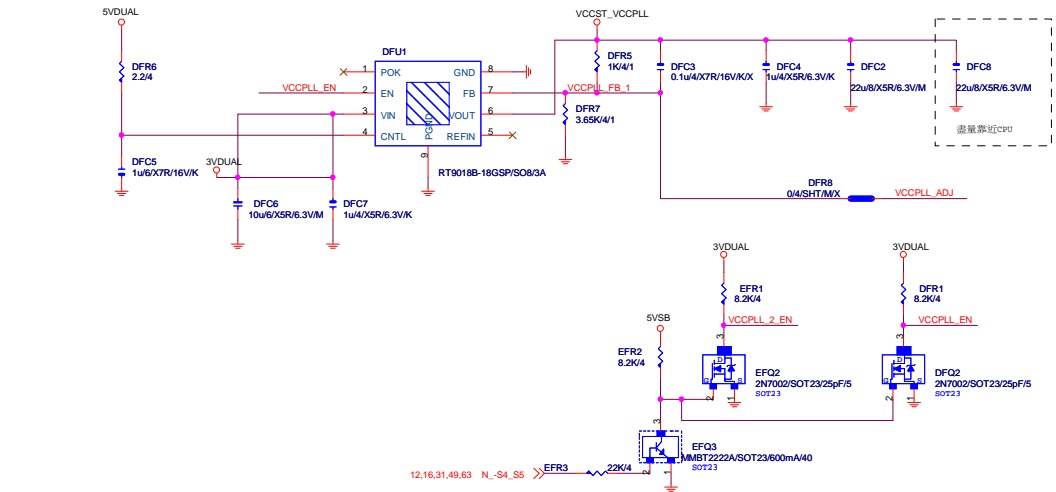


# TO USB\_DAC PORT

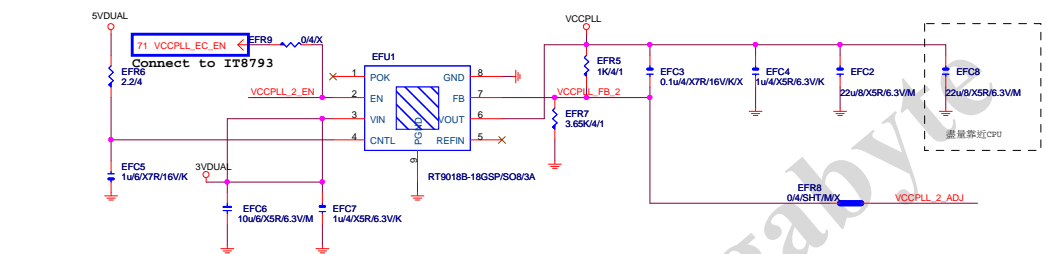
USB\_DAC5V\_J



VCCST\_VCCPLL 替換原先MOS開關線路



VCCPLL



VCCPLL\_OC

